EXPLORER XII TEST STAND DATA REDUCTION EQUIPMENT MANUAL.

BY

HAROLD H. LEVY, BRYAN R. POLSON,
PAUL HEFFNER, AND JOSEPH T. TINSLEY 1961

92 p refs

DATA INSTRUMENTATION DEVELOPMENT BRANCH
SPACE ACQUISITION DIVISION

NASA — GODDARD SPACE FLIGHT CENTER,
GREENBELT, MD.

EXPLORER XII TEST STAND DATA REDUCTION EQUIPMENT MANUAL

by
Harold H. Levy, Bryan R. Polson, Paul Heffner
and Joseph L. Tinsley
Goddard Space Flight Center

SUMMARY

The Explorer XII (1961 γ) test stand data reduction equipment is used to reduce the demodulated receiver signal to decimal form for the Explorer XII experiments at the National Aeronautics and Space Administration, the Radiation Instrumentation Design Laboratory, and the State University of Iowa.

The logic design of the equipment, the equipment itself, and the operating procedures are explained in this report. Waveform drawings, block diagrams, and schematics are included.

CONTENTS

CONTENTS (Continued)

CONTENTS (Continued)

SECTION

SECTION 1

GENERAL INFORMATION

INTRODUCTION

In order to test quickly and concisely the functioning of experiments within a satellite from the prototype period to launch time, it becomes necessary to build special purpose equipments that will reduce the satellite test experimental data immediately to a form clearly indicative of experimental results. The purpose of the Explorer XII (1961 υ) test stand data reduction equipment is to perform this function and provide the results in decimal form for the Explorer XII experiments at the National Aeronautics and Space Administration (NASA), the Radiation Instrumentation Design Laboratory (RIDL), and the State University of Iowa (SUI). In addition, the equipment will provide aspect[1] results in digital voltage form. The input to the equipment is the demodulated receiver signal.

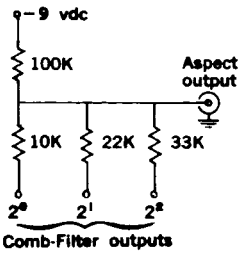
Although the equipment is primarily employed during test stand operations, it is also used during "real-time" data processing to provide "quick-look" data for the data reduction group and for the experimenters. Here, the equipment serves as a cross reference with the computer format control buffer.

EXPLORER XII SIGNAL FORMAT

In the Explorer XII satellite, the carrier wave is frequency modulated by a pulse frequency modulated (PFM) information signal so that the demodulated receiver signal presents to the data processor a straightforward Vanguard-type PFM signal. The signal consists of frames of 320 msec duration. Each frame consists of 16 channels;

[1] In the satellite there are sensors which analyze the orientation of the satellite with respect to the sun. The results of this information, referred to as "aspect", are encoded in the synchronizing burst and later decoded during reduction.

The aspect output is used during channels 0 and 1. It provides, in digital form, a voltage level indicative of the number between 0 and 7 given by the frequency within the burst. The aspect circuit is shown here. A staircase output voltage is derived from the eight possible Comb-Filter input combinations through the resistive divider network.



channel 0 is the synchronizing, or recognition channel (see Figure 1). The synchronizing channel is unique in that it has a 15-msec burst period and a 5-msec blank period, whereas the other channels have 10-msec burst periods and 10-msec blank periods.

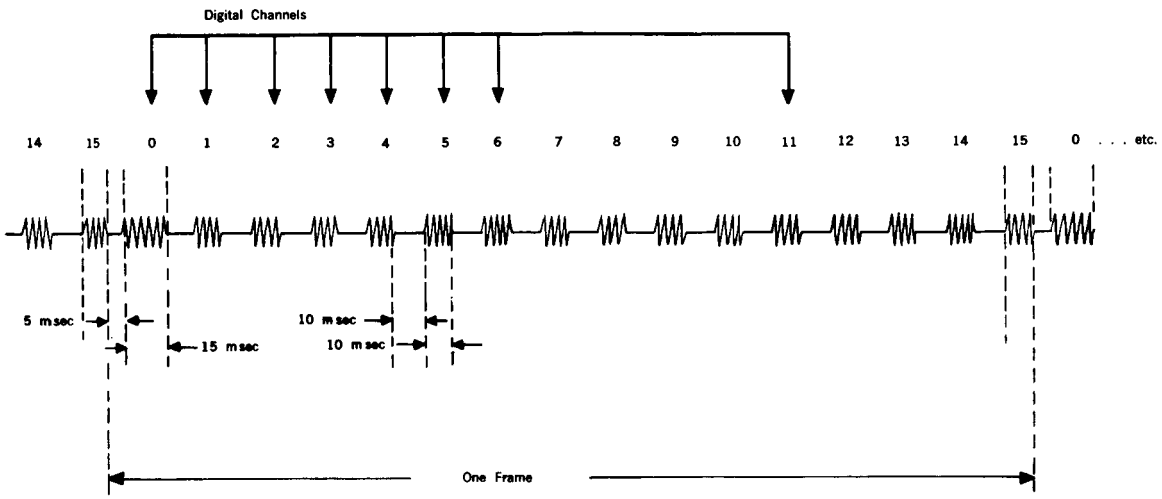


Figure 1-The sixteen channels within each frame

The information contained in channels 0, 1, 2, 3, 4, 5, 6, and 11 is digital (in the form of discrete frequencies) within the bursts of the channels. These frequencies are provided by an eight-level subcarrier oscillator in the satellite. The frequency spectrum of all eight oscillator frequencies ranges from 5 to 15 kc.

The separation and identification of channels are performed by a Decummutator. Conversion of the information from frequency to binary form is performed by the Comb-Filter where eight separate filters look for frequencies within discrete ranges. A frequency falling within the passband of a particular filter will then be represented in a corresponding binary representation, that is, as a number between 0 and 7. Recognition and reduction of the experimental data is performed in the main computer unit.

Table 1

The Relationship Between the Digital Frequencies, Binary Representation, and Decimal Representation

Frequency Limits (kc)		Binary Representation			Digital Representation
Low	High	1st 2^2	2nd 2^1	3rd 2^0	
———	<5.400	0	0	0	0
5.507	5.695	0	0	1	1
6.112	6.338	0	1	0	2
6.817	7.097	0	1	1	3
7.849	8.183	1	0	0	4
9.042	9.470	1	0	1	5
10.858	11.534	1	1	0	6
13.717	14.599	1	1	1	7

Table 1 shows the relationship between the digital frequencies, the binary representation by the Comb-Filter, and the decimal representation.

Table 2 gives the signal format of the NASA, RIDL, and the SUI experiments.

The waveform charts for the NASA, RIDL, and SUI, experiments are shown in Figures 2, 3, and 4, respectively. Figure 5 gives a waveform chart for the SUI experiment showing an expanded portion of frames 32 through 41.

Table 2

Signal Format of the NASA, RIDL, and SUI Experiments

Information	NASA Experiment	RIDL Experiment	SUI Experiment
Type of Mode	Time shared with RIDL	Time shared with NASA	Continuous Operation
Frames per unit time of sending	960 These 960 frames provide 120 words of eight frames each	320 Frames 1 through 256: 64 words Frames 257 through 320: no information, delay time only	60 frames per cycle Frames 1 through 11: provide Barker code for recognition of a new cycle Frames 12 through 32: no information, delay time only Frames 33 through 39: first word Frames 40 through 46: second word Frames 47 through 53: third word Frames 54 through 60: fourth word
Words per unit time of sending	120	64	4 words per cycle
Breakdown of frames within each word	Frames 0 through 5: storage time within the satellite Frames 6 through 8: word data and identification	All word frames contain word data	Once the cycle of four words begins, all frames contain word data

Table 2 (continued)
Signal Format of the NASA, RIDL, and SUI Experiments

Information	NASA Experiment	RIDL Experiment	SUI Experiment
Channels used and information carried	Channel 2: mode recognition by 2^1 bit; word recognition by 2^2 bit Channel 3: word data in frames 6, 7, and 8; all bits Channel 11: word data in frames 6 and 7 and identification in frame 8; all bits	Channel 2: mode recognition by the 2^1 bit; word recognition by the 2^2 bit Channel 3: word data in the 2^1 and 2^0 bits only Channel 11: word data in the 2^1 and 2^0 bits; word recognition by the 2^2 bit	Frames 1 through 11 Channel 4: Barker code Channel 5: Barker code Channel 6: Barker code Frames 33 through 60 Channel 4: word data Channel 5: word data Channel 6: word data (Two modes for encoding SUI data within channels 4, 5, and 6 were being considered by the experimenters during the early stages of the planning of Explorer XII. In order that either mode could be decoded by this equipment, logic and switches were incorporated that would enable either mode to work into the equipment.) Two modes were available, the serial mode and the parallel mode. In either mode, one data point (one 3-bit number) is provided in one frame. In the serial mode, data is provided by only the 2^0 bit, requiring all three channels (4, 5, and 6) to collectively create one 3-bit number. This new number represents a 3rd bit, a 2nd bit, and a 1st bit (2^0, 2^1, and 2^2). To the logic using this mode, channel 4 will provide the 2^0 bit, channel 5 the 2^1 bit, and channel 6 the 2^2 bit. In the parallel mode, data is provided by all three incoming bits, requiring only one channel to give a 3-bit number. In this mode, the 3-bit number is given in channel 4 and is repeated in channels 5 and 6. Only one of these channels, then, would be required to provide the SUI data contained in the frame.
Mode recognition	The 2^1 bit of channel 2 is a *one* during each frame that the NASA mode is being transmitted	The 2^1 bit of channel 2 is a *zero* during each frame that the RIDL mode is being transmitted	Barker code: the 2^0 bit of channels 4, 5, and 6 of frames 1 through 11 are in the sequence 11100010010. It is only necessary to check one channel to read this sequence.

Table 2 (continued)

Signal Format of the NASA, RIDL, and SUI Experiments

Information	NASA Experiment	RIDL Experiment	SUI Experiment
Word recognition	At the beginning of each NASA word–every eight frames–the 1st bit in channel 2 changes state (from *zero* to *one* or from *one* to *zero*).	First RIDL word: the 2^1 bit changes from a *zero* state to a *one* state during channel 2 time. Second to 64th word: the 2^2 bit of channel 11 of the last (4th) frame of the preceding word exhibits a *one* state.	The cycle of four SUI words is recognized by the Barker code and the 21 frame delay.
Word Information and Identification	By succeeding channels: 3,11,3, 11,3. Identification data is contained in the following channel 11.	By succeeding channels: 3,11,3, 11,3,11,3,11.	Serial Mode By succeeding channels (seven frames): 4,5,6, 4,5,6,4,5,6,4,5,6,4,5,6, 4,5,6,4,5,6. Parallel Mode By succeeding channels (seven frames): 4,4,4, 4,4,4,4 or 5,5,5,5,5,5,5 or 6,6,6,6,6,6,6.
Display	In decimal form: five decades for word and one decade for identification. (Time shared with RIDL)	In decimal form: six decades for word and two decades for identification. (Time shared with NASA)	In decimal form: six decades for word and one decade for identification.
Print Out	Decimal printer: one word and its identification per line. (Time shared with RIDL)	Decimal printer: one word and its identification per line. (Time shared with NASA)	Decimal printer: one word and its identification per line.

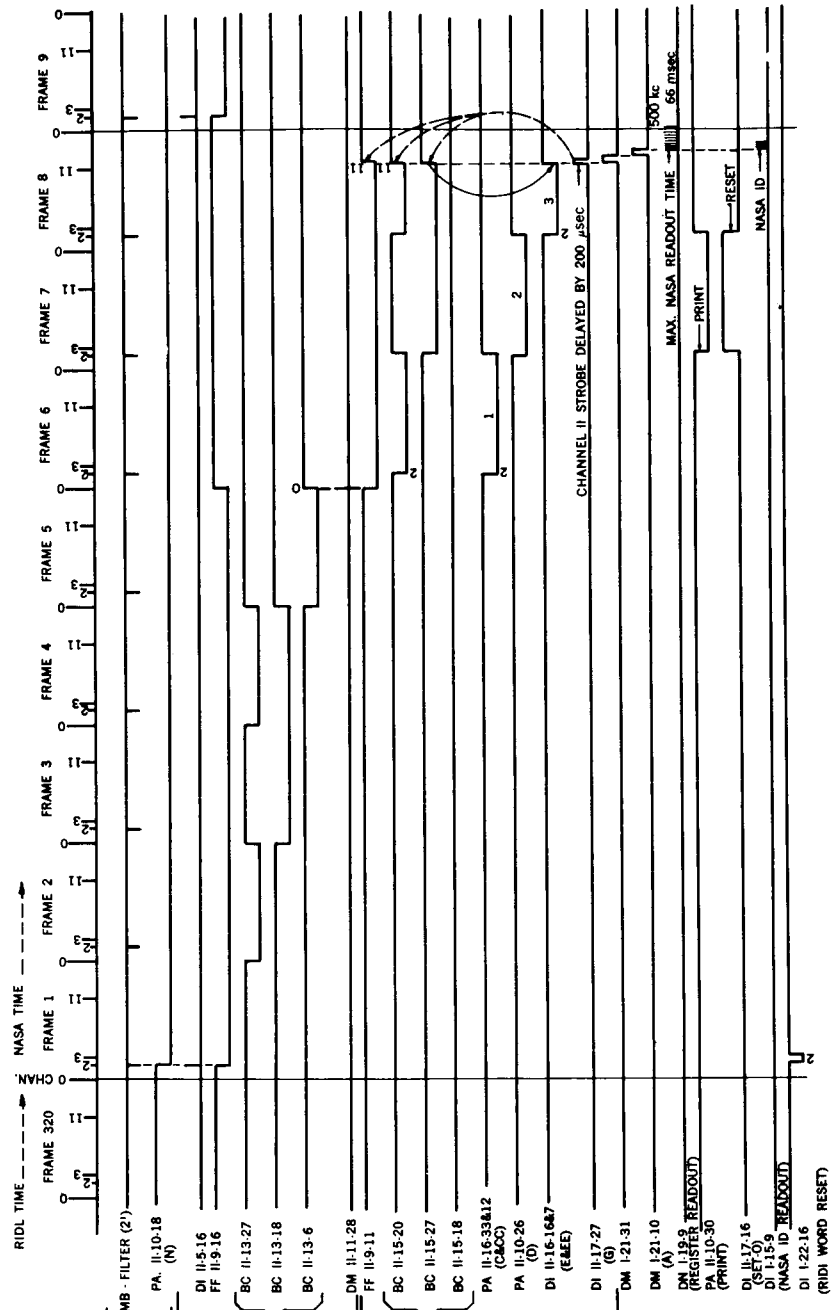


Figure 2–NASA waveform chart

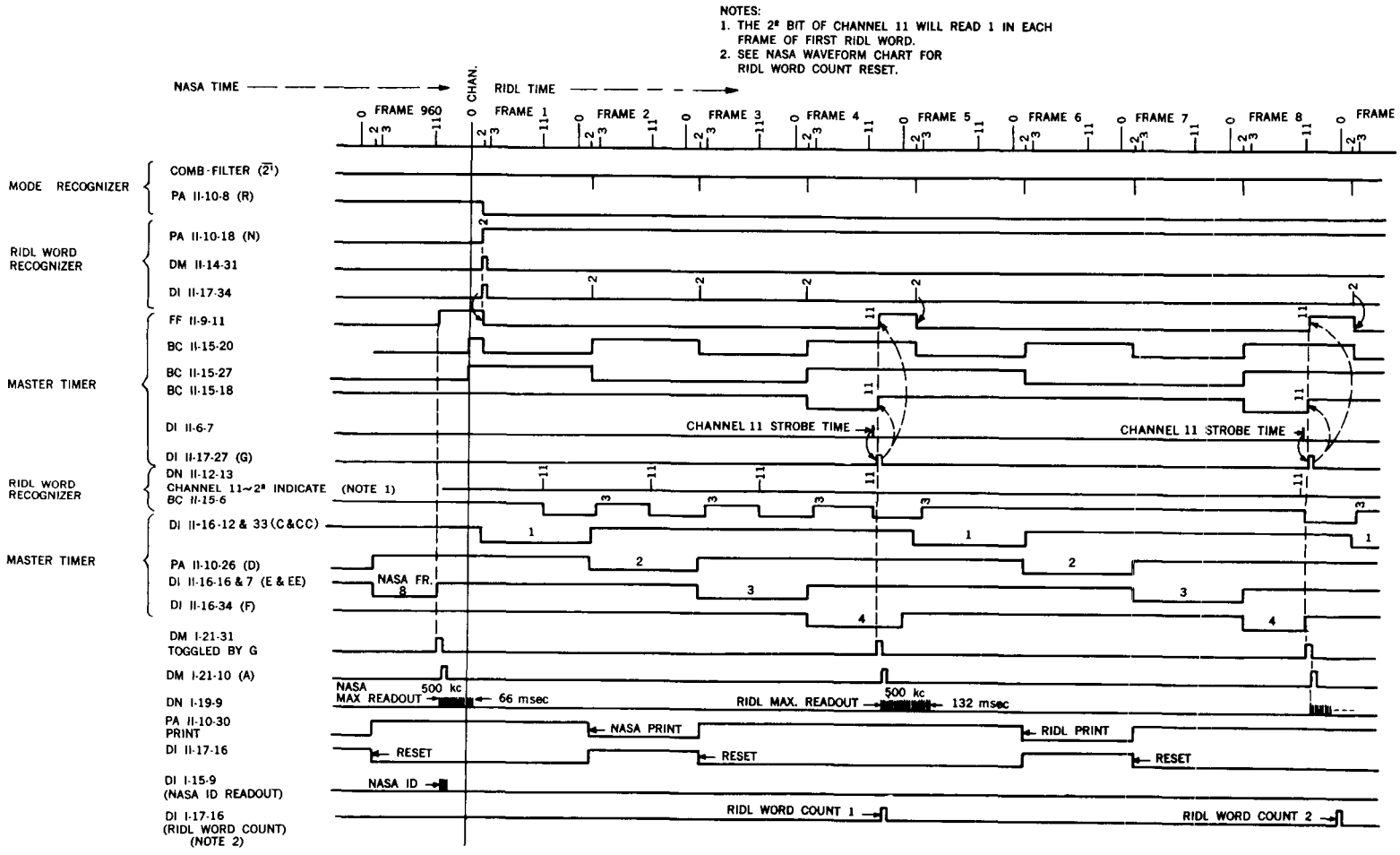


Figure 3–RIDL waveform chart

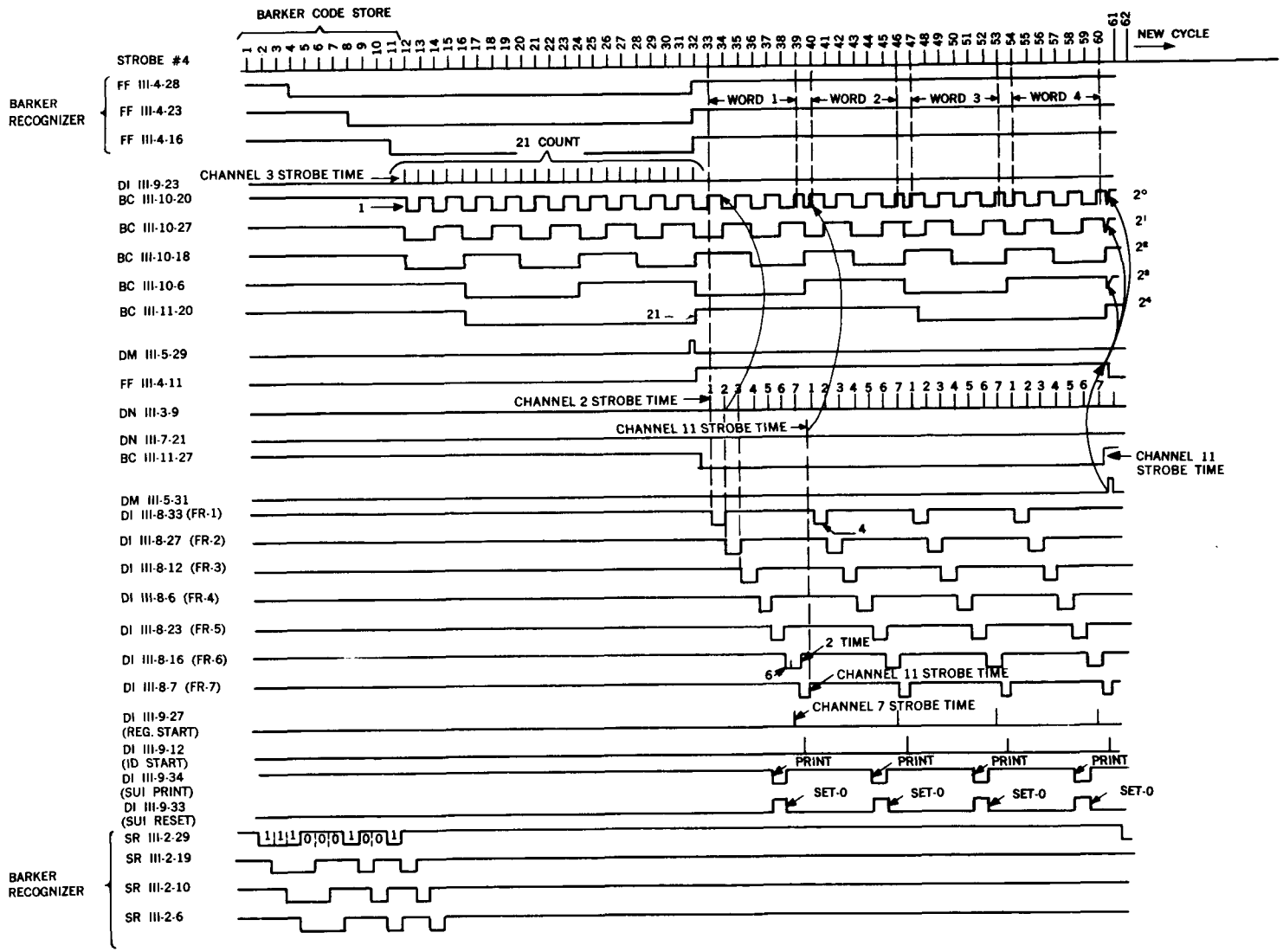


Figure 4—SUI waveform chart

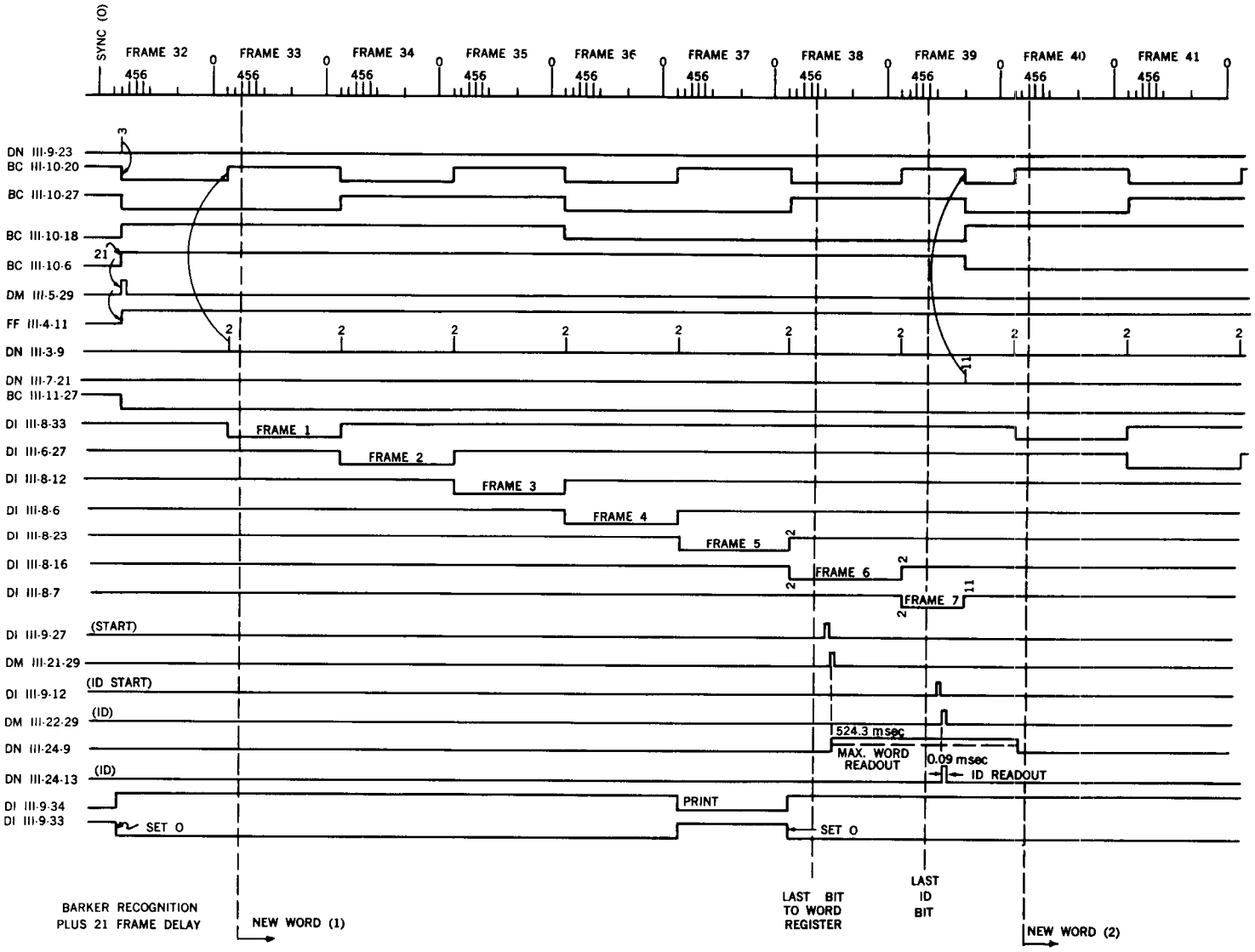


Figure 5–SUI waveform chart showing an expanded portion of frames 32 through 41

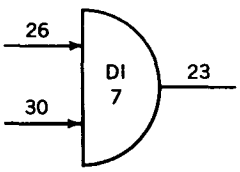
CONVENTIONS AND SYMBOLS USED IN THE DRAWINGS

The basic electronic components of the Explorer XII test stand data reduction equipment were manufactured by the Computer Control Company. The reference manual (Reference 1) supplied by this company should be used in connection with the maintenance and operation of this test stand data reduction equipment. However, the following conventions and symbols are listed so that the need to refer to Reference 1 will be reduced to a minimum. S-PAC is the designation of the series S modules used in this equipment. S-BLOC is the designation of the series S module mounting racks; there are three such racks in this equipment; S-BLOC-I, S-BLOC-II, and S-BLOC-III.

The location of the modules is given by the following code: Type of module — number of S-BLOC (in Roman numerals) — module number — output pin number. Thus, DN-III-4-8 means a NAND circuit with a diode cluster on S-BLOC-III, module 4, output pin 8. Since there are several circuits on each module, a particular circuit is identified by its output pin.

The binary representations (2^0, 2^1, 2^2, $\overline{2^0}$, $\overline{2^1}$, or $\overline{2^2}$) frequently appear on the drawings. If the binary representation 2^0, 2^1, or 2^2 appears, then the bit is true, and when this bit is in the *one* state, the voltage level will be positive. If the binary representation $\overline{2^0}$, $\overline{2^1}$, or $\overline{2^2}$ appears, then the bit is false, and when this bit is in the *zero* state, the voltage level will be negative.

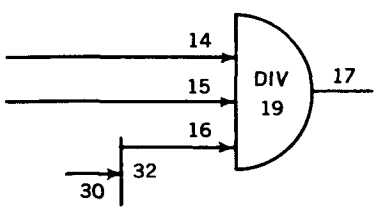
NAND circuit:



Type of module: DI
Module number: 7
Input pins: 26 and 30
Output pin: 23

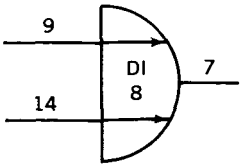
Note: in the symbol for a NAND circuit, the input arrows do NOT go through the symbol.

NAND circuit with a diode cluster



Type of module: DN
Module number: 19
Input pins: 14, 15, and 30
Outer connections: pin 32 to pin 16
Output pin: 17

NOR circuit

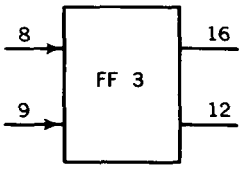


Type of module: DI
Module number: 8
Input pins: 9 and 17
Output pin: 7

Note: in the symbol for a NOR circuit, the arrows go through the symbol.

Flip-Flop circuit

The convention followed in these drawings is that the set output will be in line with the set input while the reset output will be in line with the reset input. In the example below: pin 16 is the set output, pin 8 is the set input; pin 12 is the reset output, pin 9 is the reset input.

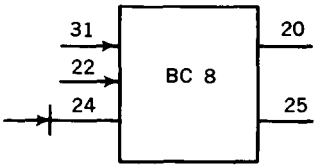


Type of module: FF
Module number: 3
Input pins: 8 and 9
Output pins: 16 and 12

Binary Counter circuit

The convention followed in these drawings is that the complementary input is always drawn to the center of the block and the set output will be in line with the set input while the reset output will be in line with the reset input. In the example below: pin 22 is the complementary input; pin 20 is the set output, pin 31 is the set input; pin 25 is the reset output, pin 24 is the reset input.

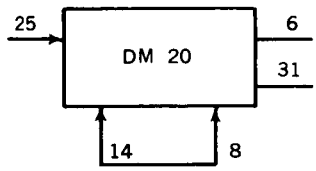
Note: the reset input requires a diode.



Type of module: BC
Module number: 8
Input pins: 22, 24, and 31
Output pins: 20 and 25

Delay-Multivibrator circuit

Because the delay-multivibrator is triggered by a positive step voltage, the convention followed in these drawings is that the output pin in line with the input pin is a negative output while the output pin not in line with the input pin is a positive output. In the example below: pin 25 is the input pin, pin 6 is the negative output, pin 31 is the positive output, and pins 8 and 14 are the internal delay capacitors. The choice of interconnected pins determines the length of the delay.

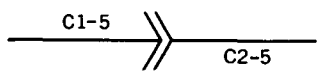


Type of module: DM
Module number: 20
Input pin: 25
Output pins: 6 and 31
Interconnections: pin 8 to pin 14 (delay 9.4 μsec)

Amphenol Connectors

Signals enter and leave the S-BLOC's by way of Amphenol connectors.

Note: signals do NOT go from S-BLOC to S-BLOC by way of Amphenol connectors.



C 1-5 means Amphenol number 1, pin number 5
C 2-5 means Amphenol number 2, pin number 5

BLOCK DIAGRAMS AND ILLUSTRATIONS OF THE EQUIPMENT

Figures 6 and 7 give general and detailed block diagrams of the equipment. Figures 8 and 9 show the front and rear view of the completed unit and Figure 10 is an enlarged view of the main control panel and the logic wiring.

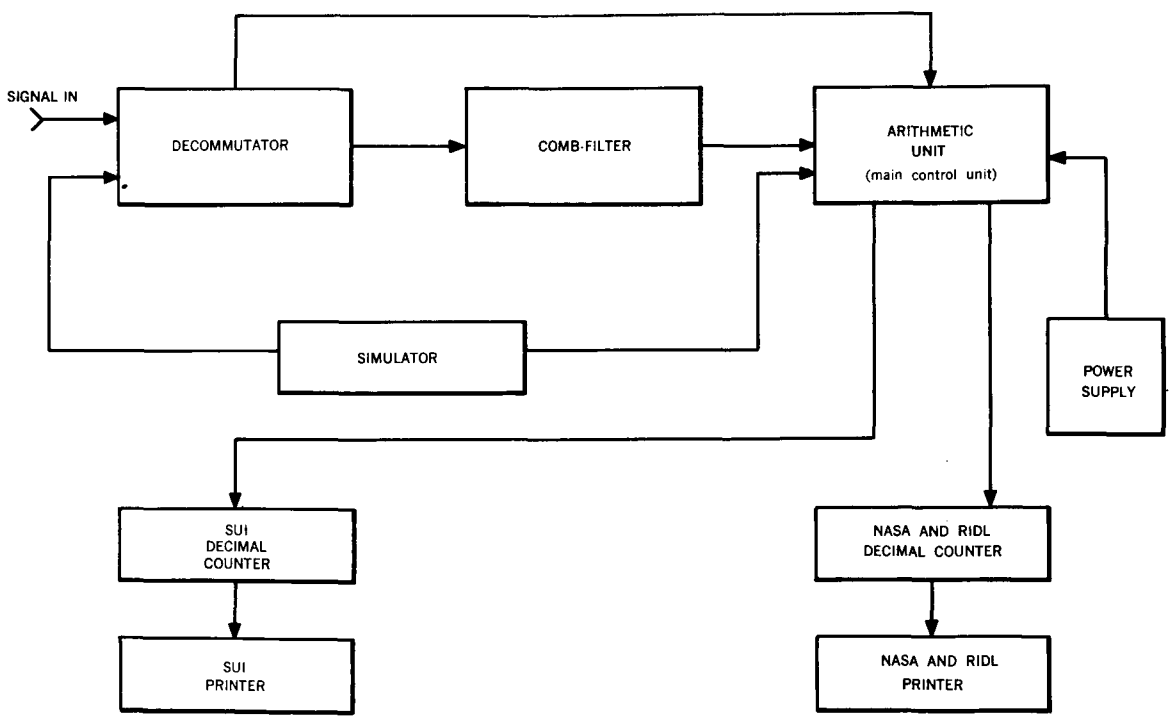


Figure 6—Overall block diagram of the Explorer XII test stand data reduction equipment

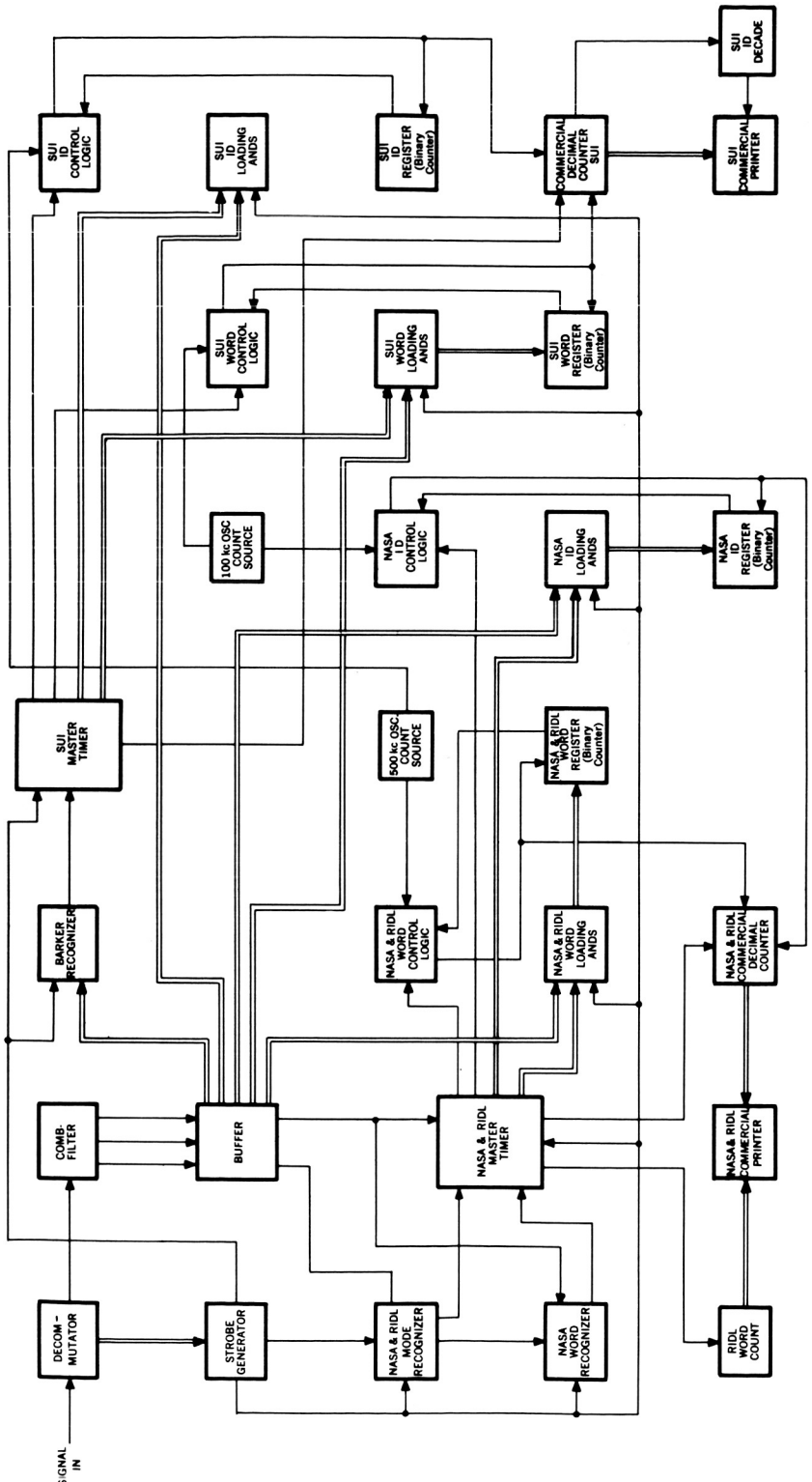


Figure 7—Detailed block diagram of the Explorer XII test stand data reduction equipment

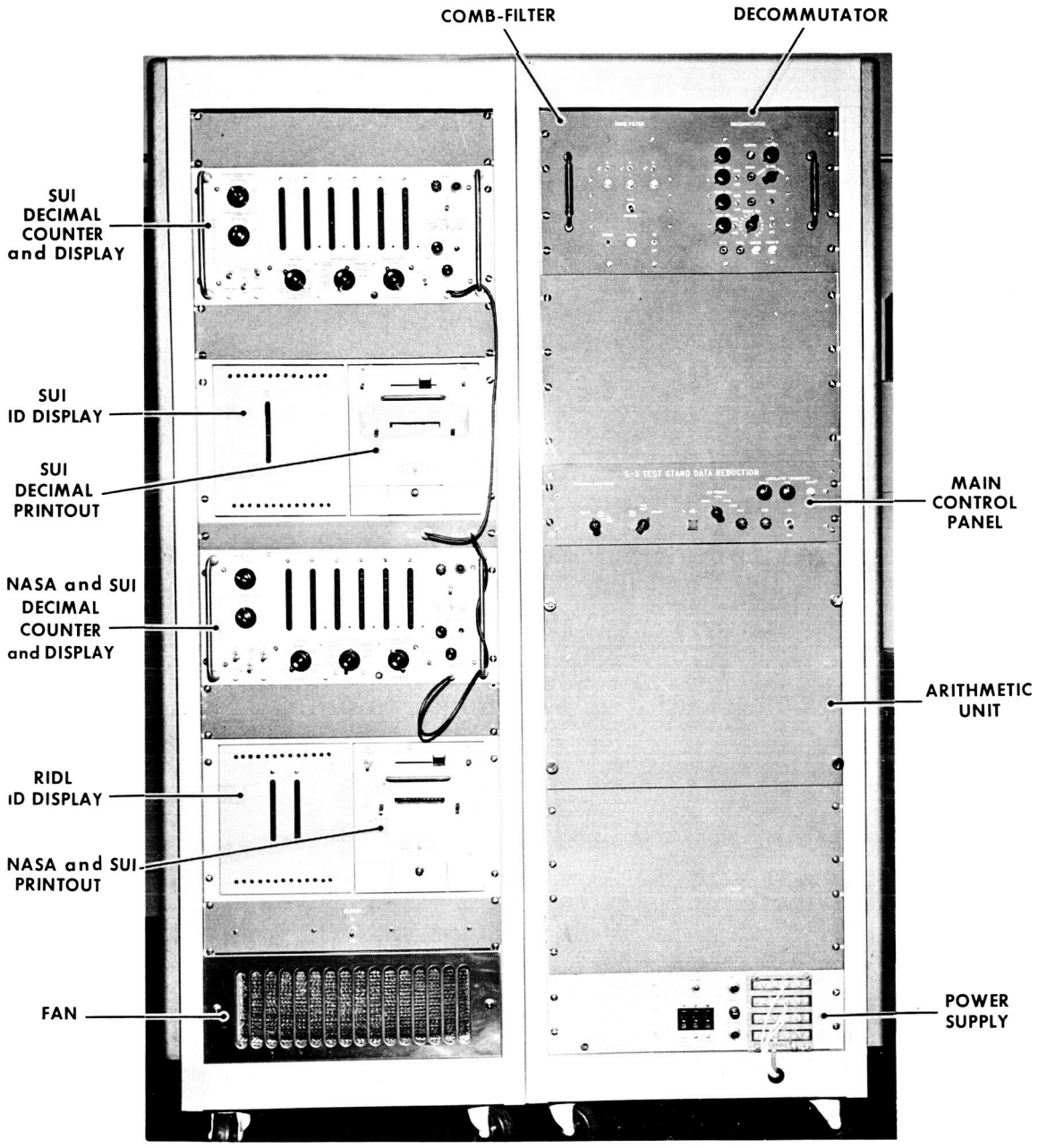


Figure 8—Front view of the complete unit

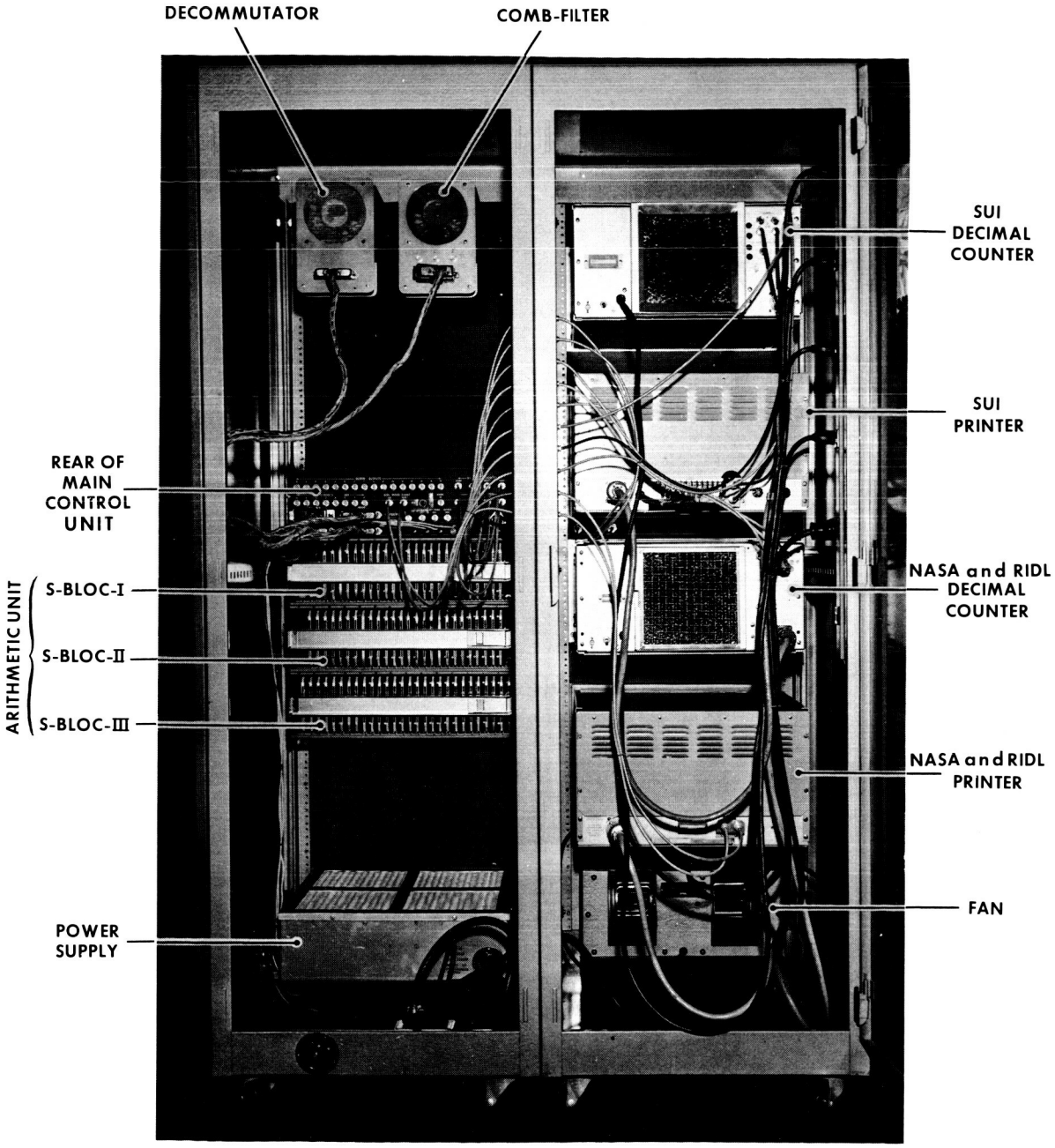


Figure 9—Rear view of the complete unit

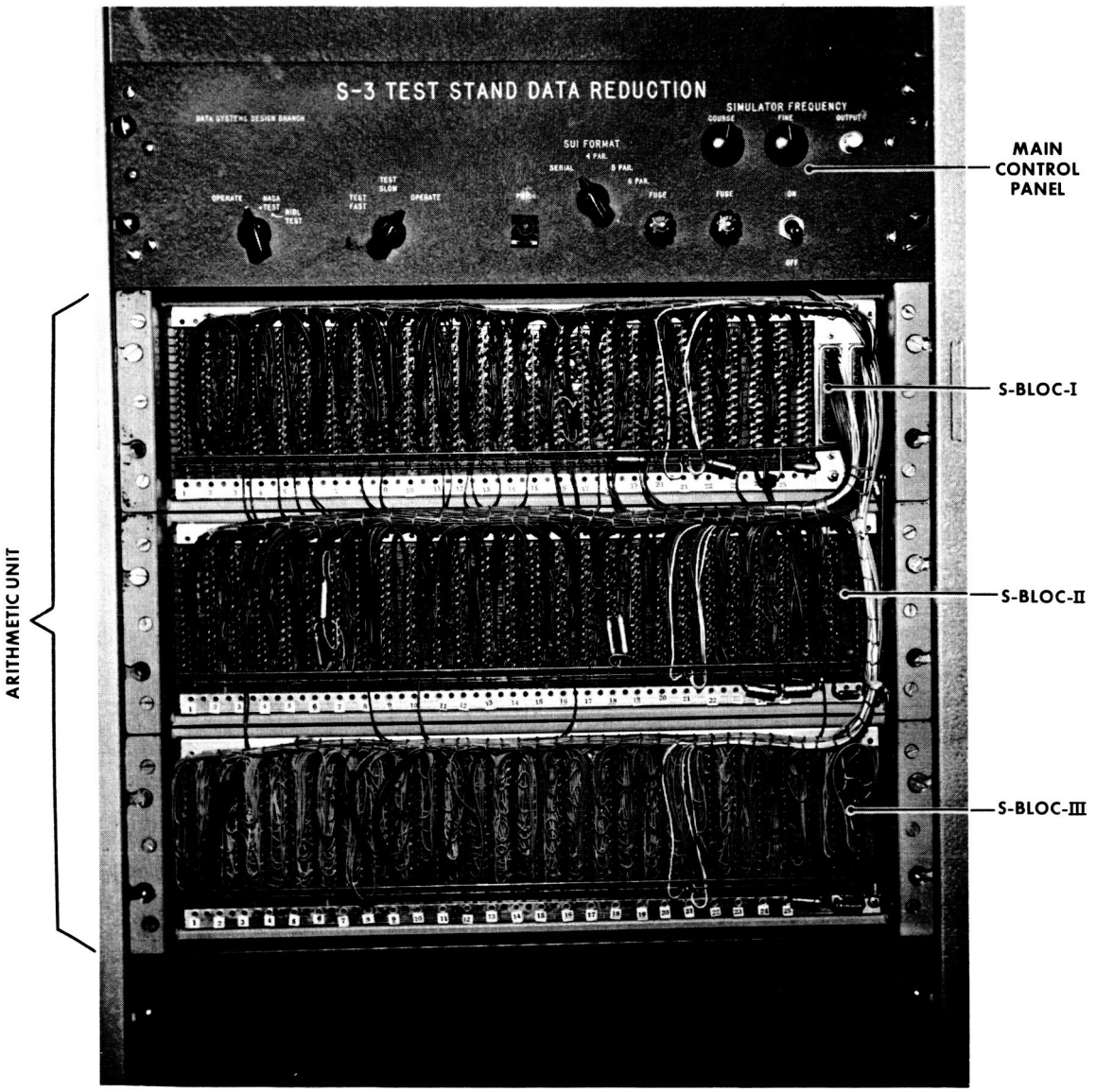


Figure 10—Enlarged view of the main control panel and the Arithmetic Unit

SECTION 2
FUNCTIONAL DESCRIPTION OF NASA AND RIDL LOGIC

GENERAL FUNCTIONAL DESCRIPTION

In order to better understand the primary functions of the NASA and RIDL logic it will be necessary to refer to the NASA and RIDL waveform charts (Figures 2 and 3) and to the general block diagram (Figure 6).

Decommutation and Detection of Frame Synchronization

The DECOMMUTATOR performs four primary functions. The first is frame synchronization. The second is the separation of each channel, providing 16 individual outputs where each output will give the detected burst of a specific channel within every frame. The third function is that of providing a continuously detected envelope of the input signal. The fourth function is automatic gain control of the raw signal before it is given to the Comb-Filter so that the Comb-Filter will see a constant amplitude signal.

Conversion of the Digitized Frequency to Binary Form

The COMB-FILTER contains eight filters, each tuned to one of the eight discrete frequencies (see page 2). A detected frequency, representing a number between 0 and 7, is shaped and then operated on by a matrix which provides a 3-bit number. Buffer stages are incorporated between the COMB-FILTER and other parts of the equipment, since the COMB-FILTER uses circuits operating at different voltage levels than circuits in the rest of the equipment.

Description of the Strobe Generator

The STROBE GENERATOR generates 10-μsec pulses that are delayed 5 msec from the beginning of the burst for each of the digital channels (except channel 1). The inputs to the STROBE GENERATOR are the individual channel outputs from the Decommutator. The STROBE GENERATOR provides a means for selecting a particular channel and

strobing the outputs of the Comb-Filter for this particular channel to determine the states of the three bits representing the information within that channel.

Detection of Mode

The NASA and RIDL MODE RECOGNIZER senses the 2^1 bit of channel 2 in order to determine which of the two time-shared experiments is being transmitted. The output of the NASA and RIDL MODE RECOGNIZER is a voltage level which is negative during the NASA mode and ground during the RIDL mode. This voltage is used to alter certain portions of the equipment so that the equipment will be in correct logical form to process the experiment being transmitted.

Recognition of Word Synchronization

The NASA word is 15 bits long and is presented three bits at a time in channels spread out over three frames. In order to collect and store this word in proper order in a register (NASA and RIDL WORD REGISTER) it is necessary to detect the beginning of a word. This is the function of the NASA WORD RECOGNIZER which recognizes changes in the 2^2 bit of channel 2 time, counts down the proper number of frames, and generates a signal which starts the Master Timer at the proper time.

The RIDL word is 18 bits long and is presented two bits at a time in channels spread out over four frames. In order to collect data, the beginning of each of the four frames must be recognized. This is done by the RIDL WORD RECOGNIZER which analyses the 2^2 bit of each 11th channel, and when this bit is in a *one* state, provides a start pulse to the Master Timer during the next frame time. This word recognizer will also indicate the beginning of an RIDL word when the NASA mode passes into the RIDL mode. This is done by detecting the time at which the 2^1 bit of channel 2 changes to a *zero* state.

Loading the Register

The problem of collecting a complete word and loading it in proper order in the register involves: (1) selection of the proper frame, (2) selection of the proper channel in that frame, and (3) sensing the binary information from the Comb-Filter occuring at that frame and channel time and placing these bits in their proper place in the NASA and RIDL WORD REGISTER. The Master Timer selects the proper frames in sequence; the Strobe Generator selects the proper channel in that frame. Signals from these two units are gated with signals from the Comb-Filter so that as the Master Timer goes through its sequence of operations a complete word is collected and loaded in the NASA and RIDL WORD REGISTER in the form of 1's complement.

Conversion of Word from Binary to Decimal; Display; and Printout

The word as collected in the register is in binary form; for quick interpretation it is necessary that it be converted to decimal form, displayed, and printed. This conversion is accomplished by supplying one count to the register (the register is a binary counter), converting 1's complement to 2's complement, and then supplying counts to the binary counter until there is an output from the last stage, which immediately gates off counts to the input. The number of counts required to generate an output from the last stage is equal to the original number – that is, before complementing. The input counts are also supplied to a commercial decimal counter and this counter is therefore loaded with the correct number in decimal form. At a time selected by the Master Timer, this number is printed and the decimal counter is set to zero in preparation for a repeat of the cycle.

The NASA and RIDL WORD CONTROL LOGIC controls the binary counter. On receipt of a start pulse from the Master Timer it inserts one count into the binary counter, opens a gate to allow counts from the 500-kc count source to be introduced into the counter, and, then, on receiving an output from the last stage of the counter, immediately gates off the input pulses. While this 500-kc signal is being gated into the NASA and RIDL Word Register the signal is being counted by the commercial Decimal Counter. The number counted during this readout of the NASA and RIDL Word Register will then be displayed as the NASA or RIDL word. With this information now stored in the decimal counter, a print command from the Master Timer, some time later, is provided to the NASA and RIDL Commercial Printer which, in turn, prints the displayed word and its identification. The commercial counters are reset after one frame time following the print command. This command is generated in the Master Timer.

It should be noted that the NASA identification bits are stored, converted to decimal form, and printed in the same manner.

DETAILED FUNCTIONAL DESCRIPTION OF THE LOGIC SUBUNITS

Decommutator

The DECOMMUTATOR is explained in Reference 2.

Comb-Filter

The COMB-FILTER is explained in Reference 3.

Buffer Stage

The COMB-FILTER BUFFER STAGE is used to work the Comb-Filter into the Arithmetic Unit because of the heavy loads that the Comb-Filter is required to drive. The COMB-FILTER BUFFER STAGE is shown in Figure 11.

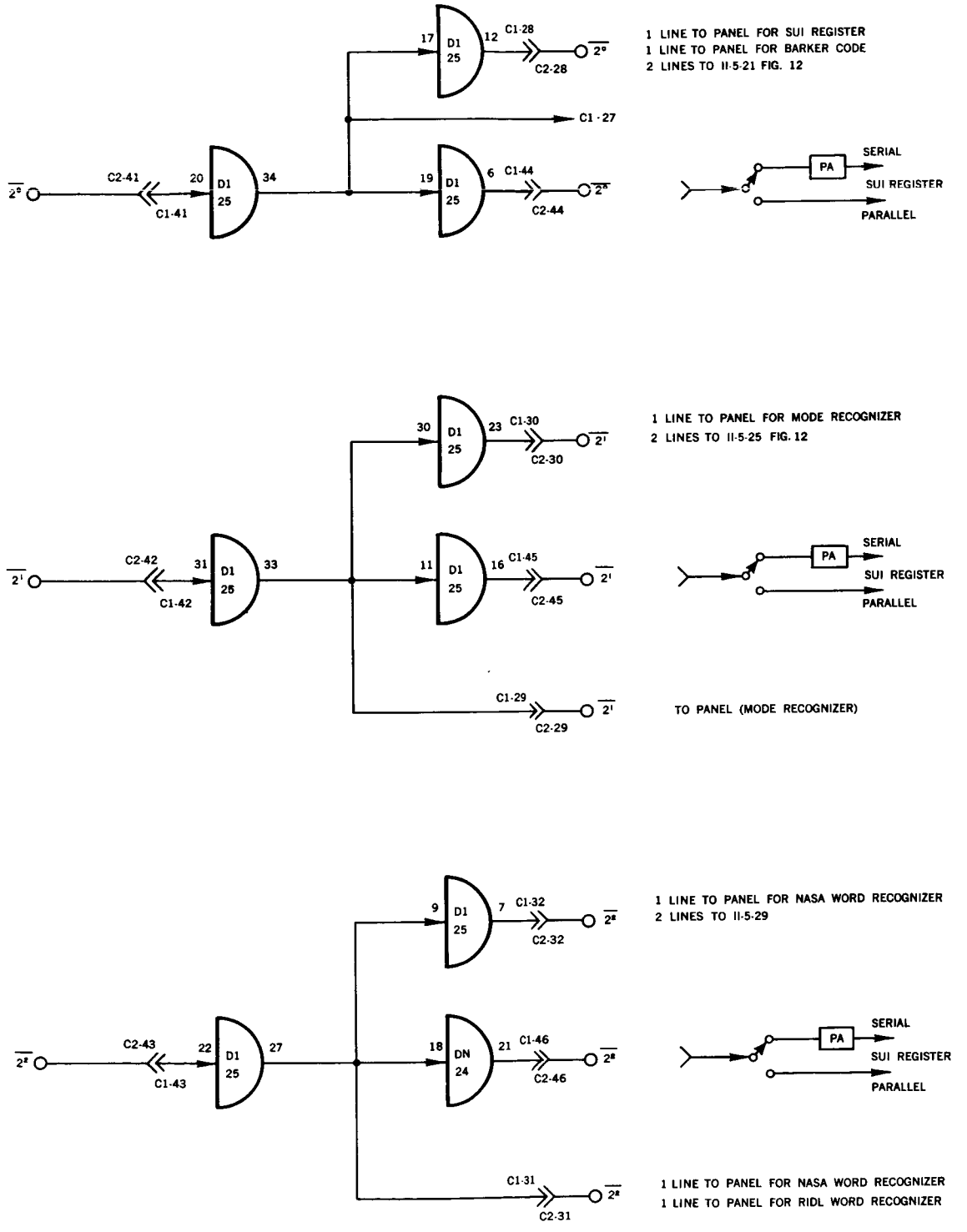


Figure 11–Comb-Filter Buffer Stage, S-BLOC-II

Strobe Generator

Refer to Figures 2 and 12. The detected envelope from the Decommutator is fed to DI 8-34 which functions as an inverter. The inverted waveform is then supplied to DM 7-31, a monostable multivibrator set to generate a 5-msec pulse. This output is then inverted and fed to DM 7-28 which has been set to generate a 10-μsec pulse. Thus, at the output of DI 8-27, an inverter, there will be a train of negative-going 10-μsec pulses occurring in the middle of every burst time, approximately 5 msec after the beginning of each burst. These pulses are supplied to eight inverting NAND gates which have as gating inputs the separated envelopes for channels 0, 2, 3, 4, 5, 6, 7, and 11, respectively. The logic block DI 3-34 has as an output a positive-going 10-μsec pulse occurring only during channel 0 time and 5 msec after the beginning of the channel 0 burst. The same is true for the other seven channels; DI 3-33 will have a 10-μsec pulse output during channel 1 time, and so on for the other channels. All strobes are fed through inverters in parallel in order to split a large load.

The switch SW-1 is used to change the time constant for DM 24-29 to allow a Test Fast-Test Slow mode. In the Test Fast mode, outputs K, L, and M are binary information from the Comb-Filter which has been NAND'ed with channel 3 strobe. The outputs P, Q, and S are binary information NAND'ed with channel 11 strobe.

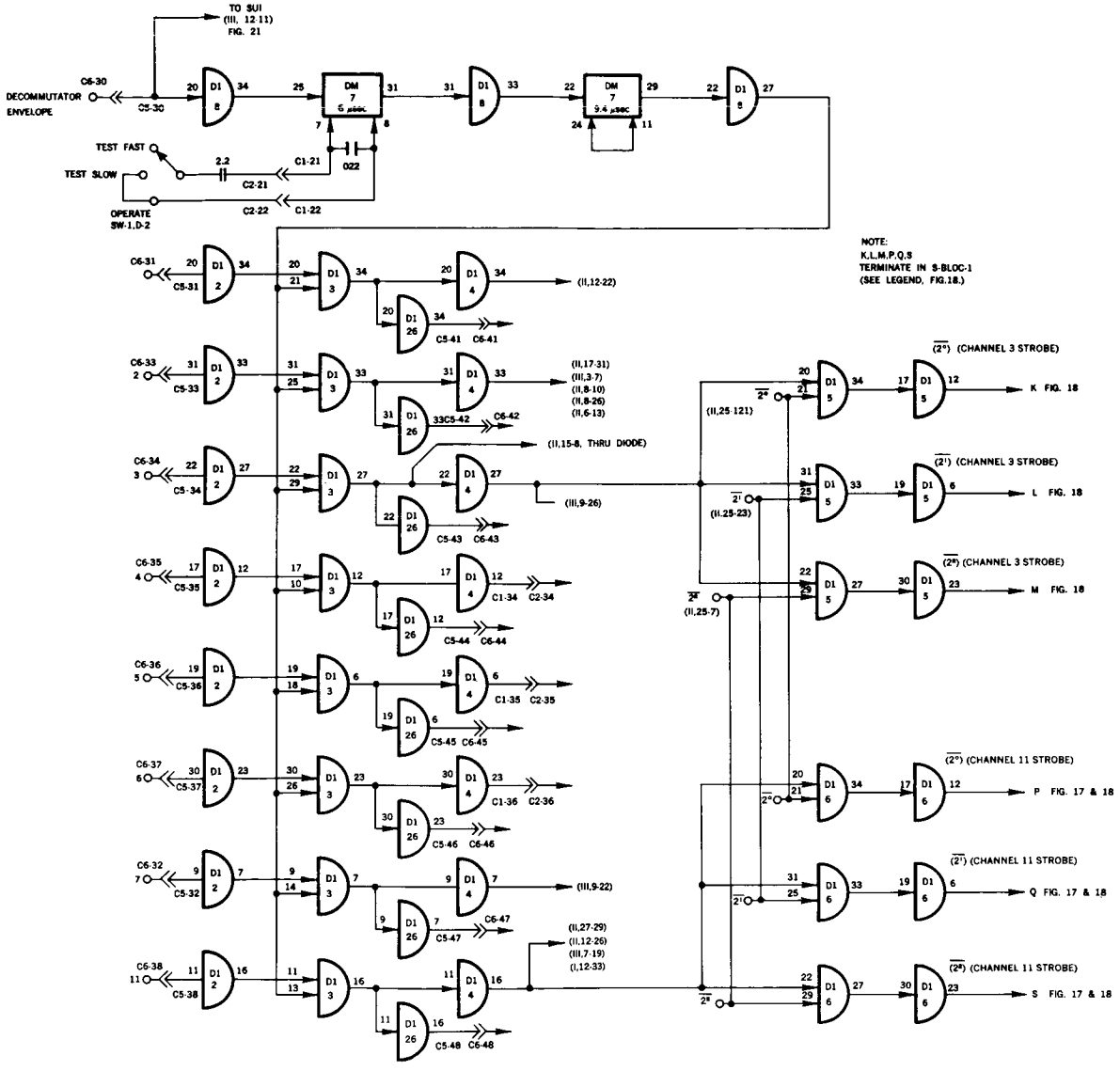


Figure 12–Strobe Generator, S-BLOC-II

Mode Recognizer

The function of the MODE RECOGNIZER (Figures 2 and 13) is to provide a gating voltage which is at -6 volts during the 960 frame NASA interval and at 0 volts during the 320 frame RIDL interval. The Explorer XII format provides the 2^1 bit of channel 2 as a recognition signal separating the two time-shared experiments. A switch SW-2 is provided to allow the equipment to be held continuously in the NASA or RIDL mode for servicing and checking. With SW-1 and SW-2 in the Operate position, the 2^1 bit is applied to DI 8-12 and $\overline{2^1}$ is applied to DI 8-6. The Channel 2 strobe is also supplied to both of these NAND gates. During the time that this 2^1 bit is a *one* state (-6 volts), DI 8-12 is gated on and will have an output at channel 2 strobe time. This output sets FF 9-28 to -6 volts on pin 28. The flip-flop remains in this state until the 2^1 bit changes to the *zero*, at which time there will be an output from DI 8-6 setting the flip-flop to its other state. Logic blocks PA 10-8 and PA 10-18 are impedance matching devices and inverters.

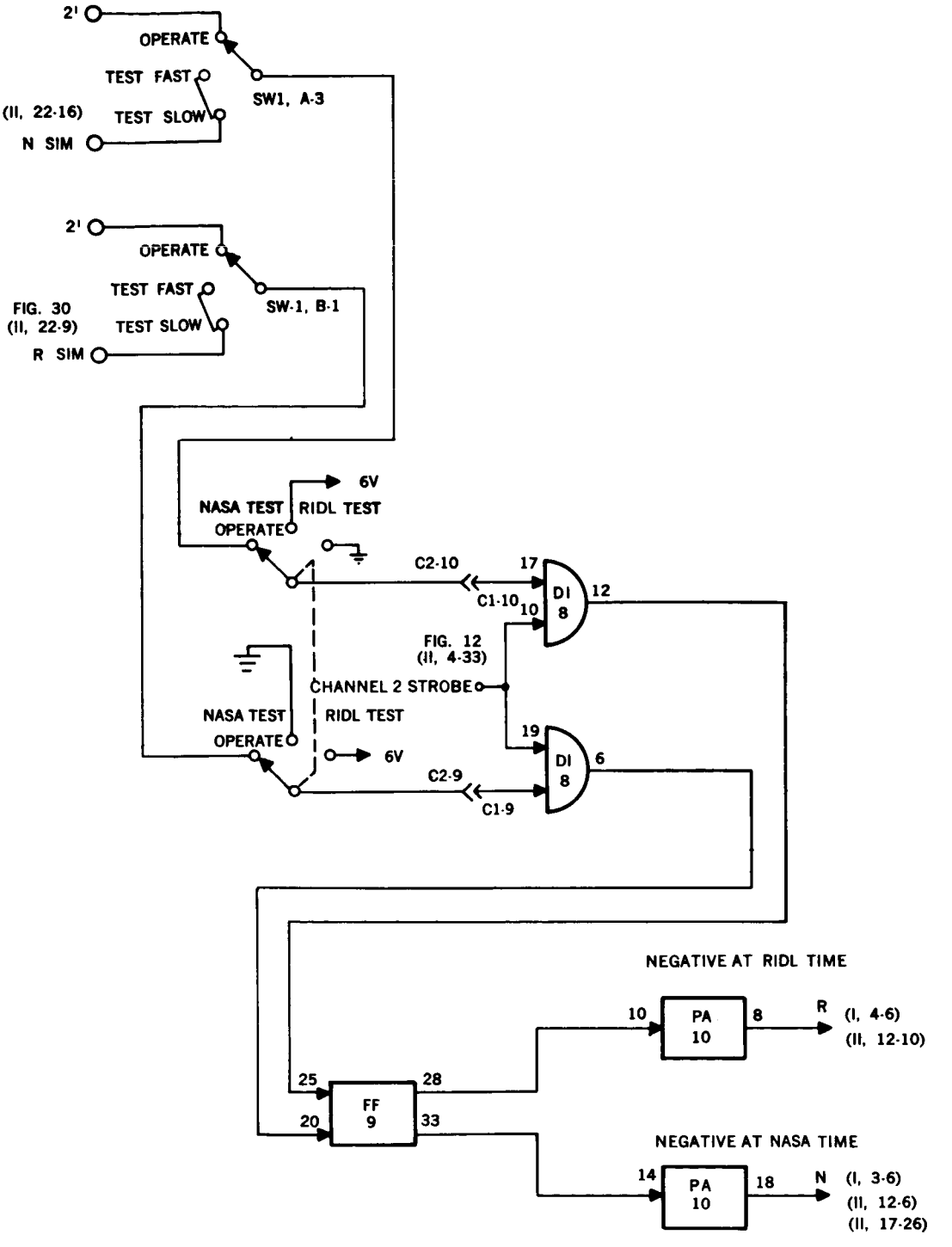


Figure 13–NASA and RIDL Mode Recognizer, S-BLOC-II

NASA Word Recognizer

The NASA WORD RECOGNIZER (Figures 2 and 14) recognizes the beginning of the eight frame NASA experiment interval, counts down five frames, and, at frame 6 channel 0 time, delivers a start signal to the Master Timer logic. The NAND gate DI 8-23 has an output at channel 2 strobe time during the eight frames that the 2^2 bit is a *one* state; DI 8-16 has outputs when the $\overline{2^2}$ bit is a *one* . Therefore, FF 9-23 will change state every eight frames. The two multivibrators DM 11-31 and DM 11-29 fire on the positive going edge of a waveform. Logic block DI 8-7 is a NOR circuit; DI 8-33 is an inverter and delivers a pulse every eight frames at frame 0 of the eight frame interval. This pulse sets FF 9-16 to the state that gates on DN 12-9 (a NAND gate) and allows channel 0 strobe pulses to be applied to the count-by-five counter. (It should be noted that DN 12-9 is also gated at pin 6 with N, the output of the Mode Recognizer.) The output of the last stop of this counter fires DM 11-28 frame 6 channel 0 strobe time. This pulse starts the Master Timer and resets FF 9-16 in preparation for a repeat of the cycle.

The NASA WORD RECOGNIZER is gated off by N on pin 6 of DN 12-9 during the RIDL mode.

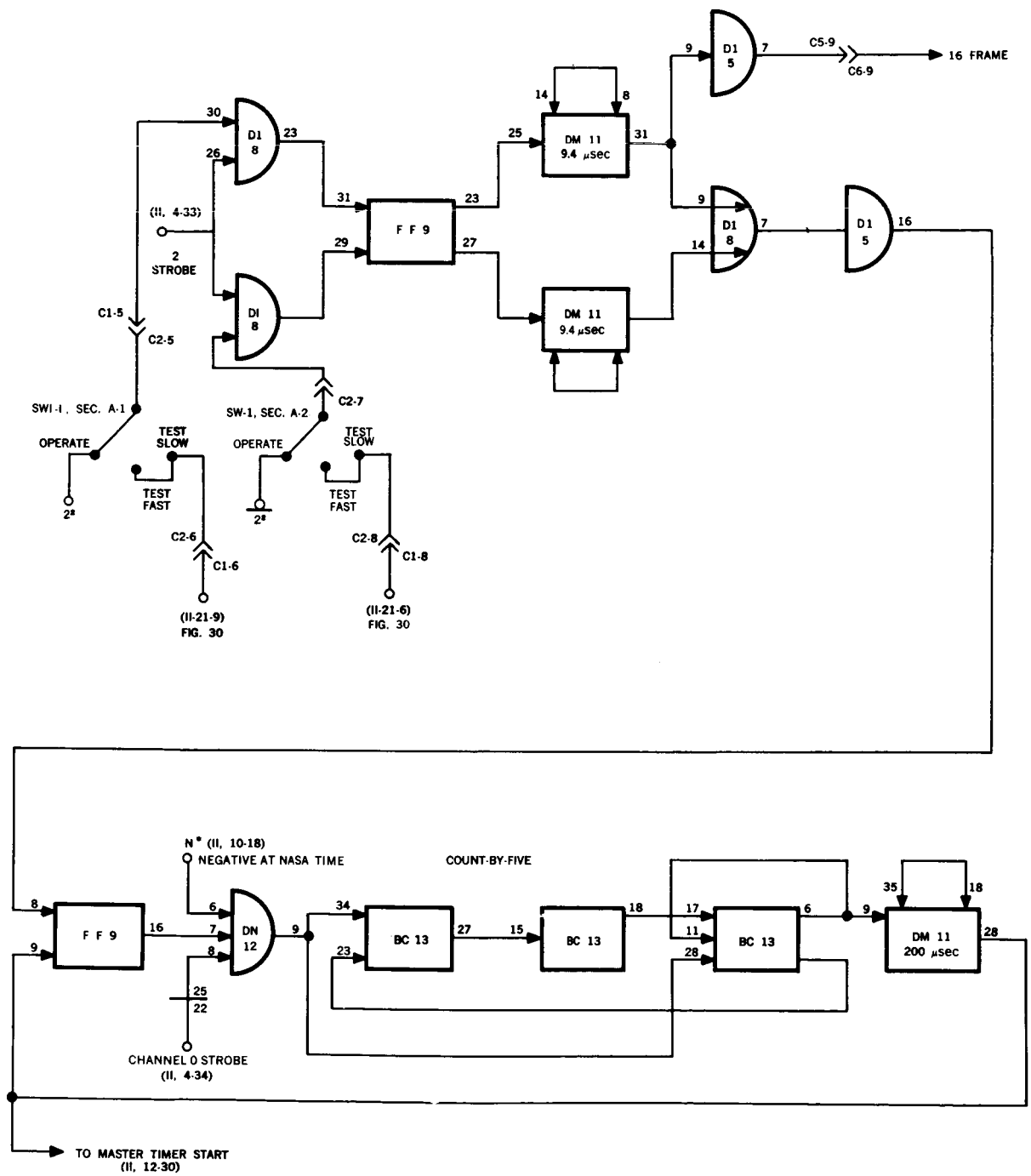


Figure 14–NASA Word Recognizer, S-BLOC-II

RIDL Word Recognizer

Refer to Figure 15. The RIDL WORD RECOGNIZER (Figure 15) supplies a start pulse to the Master Timer during the RIDL mode. Logic block DN 12-13 is gated on by R at pin 10 during the RIDL mode (and off during the NASA mode). There will be an output from DN 12-13 only during the RIDL mode and when the 2^2 bit is a *one* (negative) during channel 11 strobe time. This will be at frame 4 channel 11 of the four-frame RIDL interval. The output pulse sets flip-flop BC 15-5 to the mode which gates on DI 1-16. The next channel 2 strobe appears at frame 0 channel 2 time and will pass through this NAND gate. This output is applied to NOR gate DN 12-17 and serves as a start pulse for the Master Timer. It should be noted that the flip-flop BC 15-6 is reset at frame 0 channel 3 time in preparation for a repeat of the cycle.

The logic works in all cases except for the first RIDL word. In this case, DM 14-31 is triggered by the output N from the Mode Recognizer and supplies a start pulse to the Master Timer.

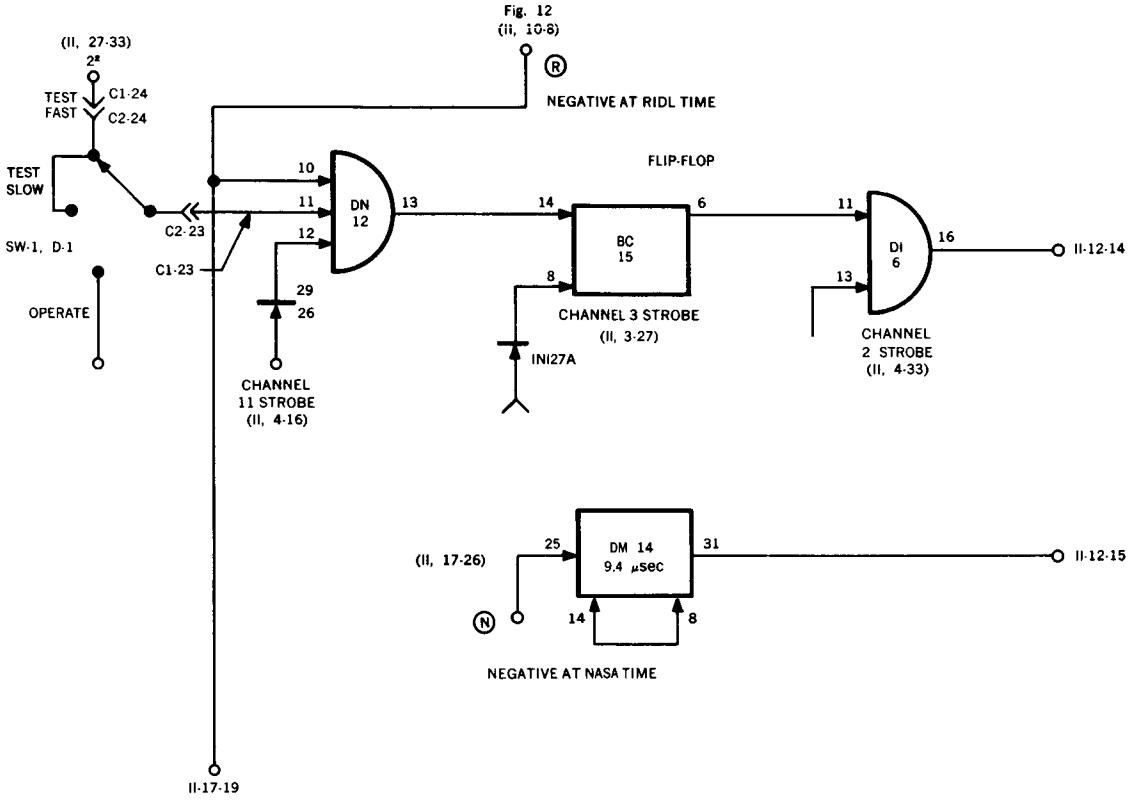


Figure 15—RIDL Word Recognizer, S-BLOC-II

Master Timer

THE NASA MODE

Refer to Figures 2 and 16. A pulse (labeled Master Timer start) generated as an output from the NASA Word Recognizer and occurring at the frame 6 channel 2 strobe time is introduced into a NOR circuit DN 12-17. This pulse is inverted and sets FF 9-11 to the state which gates on NAND circuit DI 17-33. The channel 2 strobe pulse is thus introduced into the three-stage binary counter (BC 15-20, BC 15-27, and BC 15-18). The first count introduced, at the frame 6 channel 2 strobe time, places this counter in the state which gates on NAND circuit DI 16-27. The second count, at frame 7 channel 2 strobe time, gates off DI 16-27 and gates on DI 16-6. The third count gates off DI 16-6 and gates on DI 16-23. Figure 2 shows waveforms at points C, CC, D, E, and EE.

The voltage at EE gates on NAND circuit DI 27-27 and allows the frame 8 channel 11 strobe to fire DM 25-31 Logic blocks DM 25-31, DI 27-23, and DM 14-17 form a delay circuit which generates a 9.4-μsec pulse delay 200 μsec from the frame 8 channel 11 strobe. The point labeled N gates on NAND circuit DI 17-23 during the NASA mode only and allows this delayed pulse to go through NOR DI 17-12 and inverter DI 17-27 to the reset points of the binary counter, setting this counter to *zero*. This same pulse sets FF 9-11 to the state, gating off DI 17-33. The MASTER TIMER has now completed its cycle and will repeat this cycle upon receipt of the next Master Timer start pulse.

Logic blocks DI 16-33 and DI 16-12 are inverters in parallel. Two inverters are used at this point in order to split a large load. The same is true of DI 16-6 and DI 16-7. Similarly, the power amplifier PA 10-30 is used for impedance matching.

The output of PA 18-30 at pin 30, labeled NR print, is used to initiate a print command to the decimal counter to store the processed word from the preceding cycle of processing. This is true in both the NASA and RIDL mode.

THE RIDL MODE

Refer to Figures 3 and 16. In this mode, the MASTER TIMER is started by a signal from the RIDL Word Recognizer. The action is the same as described for the NASA mode up to the point of generating the reset pulse. Logic block DI 17-23 is gated off by input N, and, therefore, the reset pulse is not available from this source. The MASTER TIMER then continues to run, gating off DI 16-23 and gating on DN 12-21. Logic block DM 18-28 is fired at frame 4 channel 11 time. Logic block DI 17-6 is gated on by R from the Mode Recognizer allowing the reset pulse to be applied to the counter and FF 9-11 at this time (frame 4 channel 11 strobe time) delayed by 200 μsec.

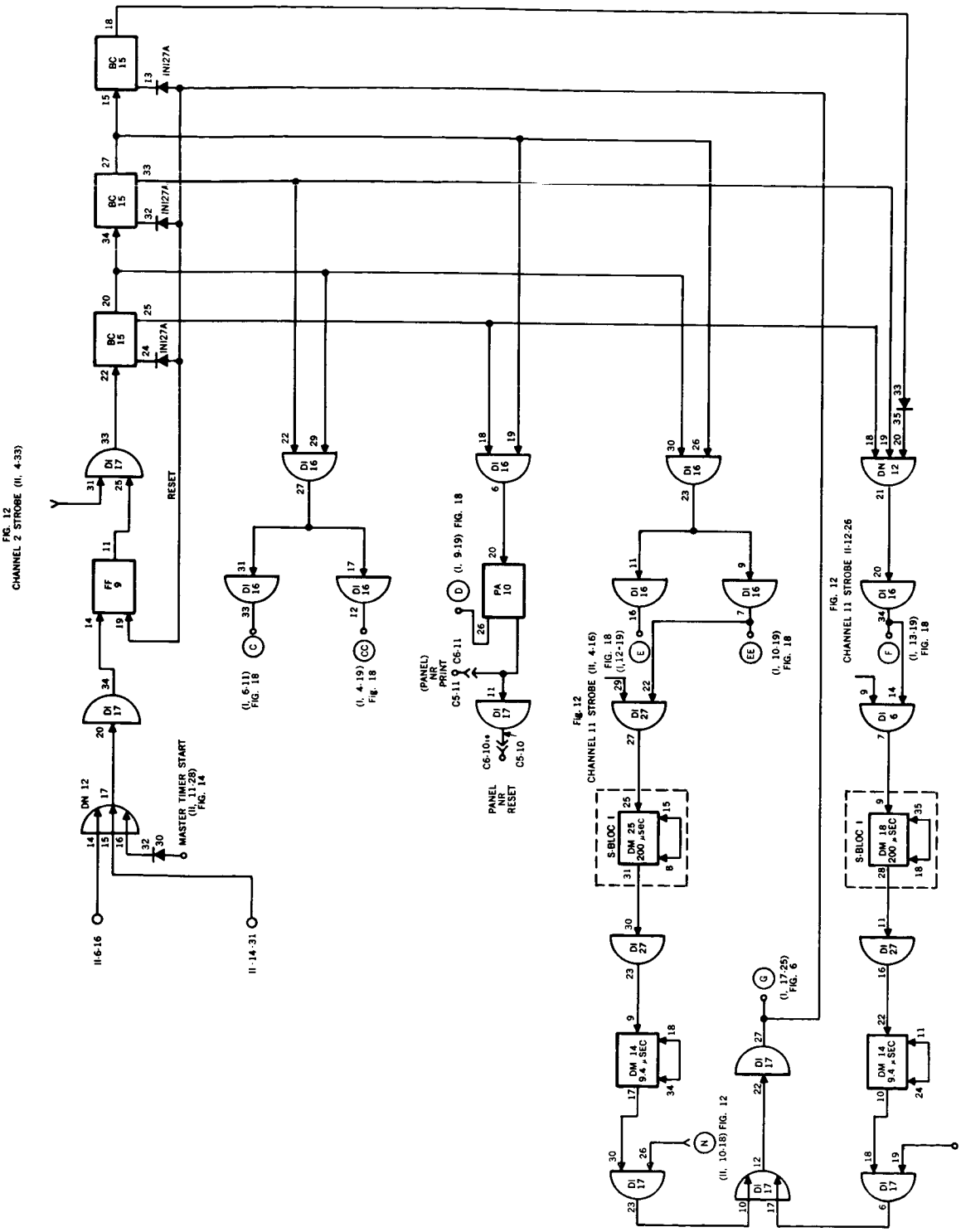


Figure 16–Master Timer, S-BLOC-II

NASA Identification, Binary to Decimal Conversion

Refer to Figures 2 and 17. The three loading NAND's DN 15-13, DN 15-17, and DN 15-21 are gated on by the input marked N (from the Mode Recognizer) during the NASA interval and gated off during the RIDL interval by this same input. The input marked "E" comes from the Master Timer and gates these three NAND circuits on during frame 8 channel 11. The input marked "P" is the state of the 2^0 bit as seen at channel 11 strobe time, "O" is the state of the 2^1 bit as seen at channel 11 strobe time and "S" is the state of the 2^2 bit as seen at channel 11 strobe time. Thus, at frame 28 channel 11 time (NASA identification word time) the three stage binary counter is loaded with the 1's complement of the NASA identification word. The input marked "G", a pulse from the Master Timer, appears after the loading process is completed. This pulse is introduced as one count into the binary counter through NOR circuit DI 22-12 and inverter DI 22-6. The counter is now loaded with the 2's complement of the identification word. Logic blocks DM 21-31, DI 22-34, and DM 21-10 function as a delay circuit to furnish a pulse 9 μsec wide occurring 15 μsec after G. This pulse starts the countout and is delayed to allow the previously mentioned one count to be registered before the countout begins. The delayed start pulse is applied through DI 22-23 to FF 20-27, throwing this flip-flop to the state which gates on DI 22-27 and DN 15-9. (The function of DM 21-28 will be explained later; at this point, it will suffice to say that it is quiescent and in a state which gates on DI 22-23.) Logic block DN 15-9 is now gated on at pin 6 and has applied at pin 7 a 100-kc square wave from MV 23-6. If the input at pin 22, DN 15-9, were eliminated, then the desired end would be achieved; that is, counts would be introduced into the binary counter on signal from the start pulse G. However, since G and the 100-kc square wave are not synchronized, the first pulse from DN 15-9 would be a partial pulse of varying width and in some cases would cause a partial, or silver, output from the multivibrator DM 25-29. The logic performed by DI 22-23, DI 22-27, and FF 20-33 is to eliminate the possibility of this partial first pulse. The flip-flop FF 22-33 will throw to the state gating on DN 15-9 at pin 22 only when both: (1) FF 20-27 has thrown to the state gating on DI 22-27, and (2) MV-6 is in the positive portion of its cycle. Logic block DN 15-19 will now pass the next negative-going pulse from MV 23-6. An analysis of this action shows that a full width first pulse is guaranteed.

The output of DN 15-9, a 100-kc square wave, fires DM 25-29 at a 100-kc repetition rate. This is supplied to the NASA identification decade on a commercial decimal counter, and at the same time is supplied to the three-stage binary counter through DI 22-12 and DI 22-6. Since the binary counter has been preset to the 2's complement of any number

n, the same number of pulses (n) will be required to generate an output from the last stage. This output fires DM 21-28 and, on the leading edge of the 200-μsec pulse from this multivibrator, FF 20-27 is thrown to the state which gates off DN 15-9. By this method the commercial decade counter is loaded with n, the NASA identification number.

Logic block DM 25-29 is necessary in order to guarantee a full width last pulse. Without this multivibrator, that is, if the output of DN 15-9 were supplied directly to DI 22-12, the last pulse would have a width equal to the delay in the three-stage binary counter plus the delay in DM 21-28 and FF 20-27. The logic to guarantee full width pulses was included to avoid generating a pulse which might trigger the binary counter without triggering the commercial decimal counter, or vice versa.

Logic block DM 21-28 at the end of the binary counter chain was included for two reasons: First the binary counter and flip-flop are dc coupled on both input and output and if these two had been coupled directly together, the flip-flop FF 20-27 would have been held in the state dictated by BC 14-18, rather than being free to respond later to an input from DI 22-23. Logic block DM 21-28 forms a pulse in order to avoid this difficulty. Secondly, this multivibrator nullifies a difficulty associated with the unique cause of the NASA identification number being zero. In this case there is an output from the last stage when the one count is inserted at G time and, since the start pulse A is delayed from G, A will occur after an output from the last stage of the binary counter. Without some correction, the logic would go through another complete cycle and the number printed would be 8 instead of 0. The 200-μsec pulse from DM 21-28 inhibits DI 22-23 and prevents the start pulse A from throwing FF 20-27 in this unique case.

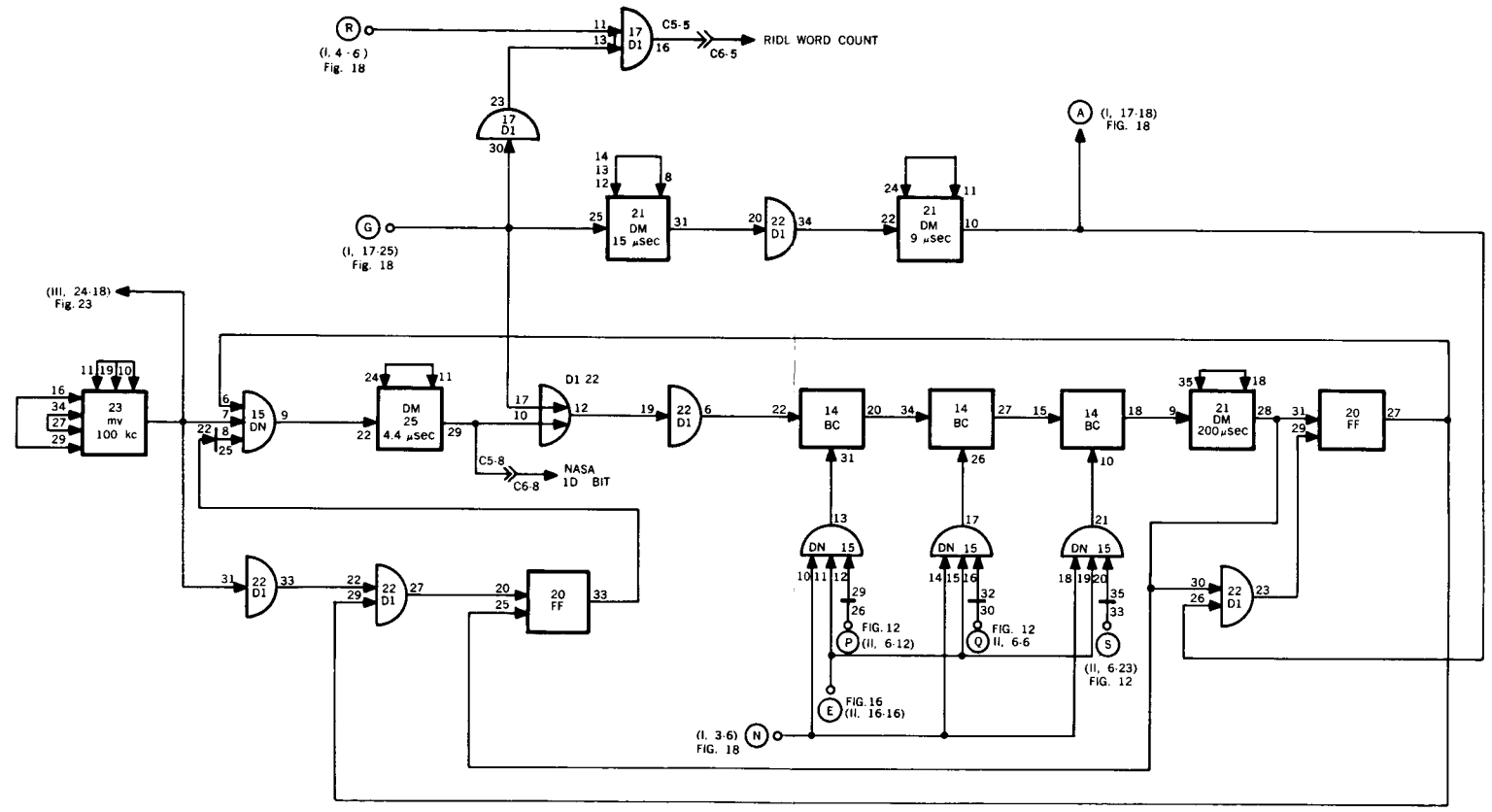
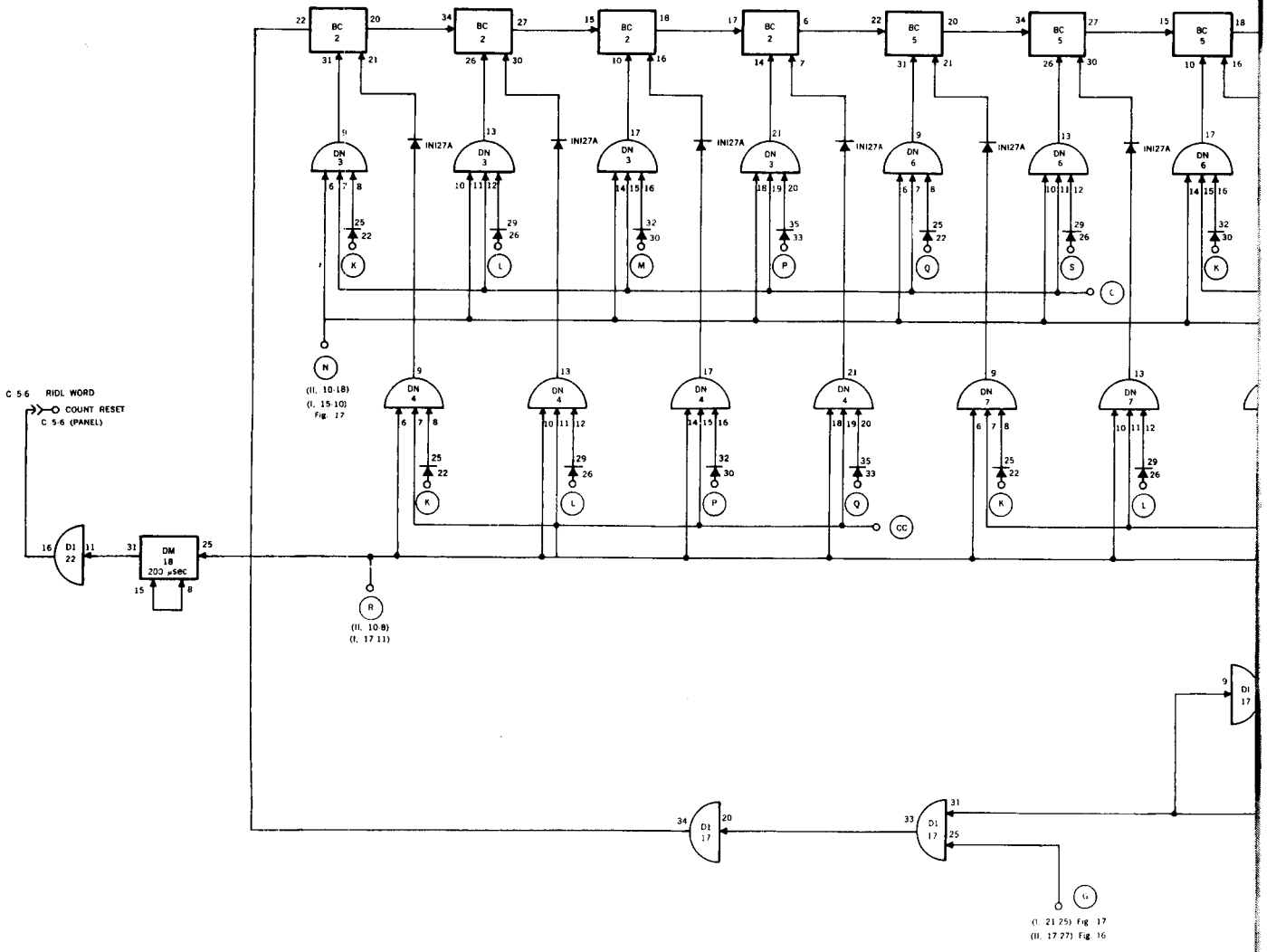


Figure 17—NASA and RIDL identification binary counter and control, S-BLOC-I

NASA and RIDL Binary Counter and Control Logic

Refer to Figures 2 and 18. The logic in this unit is almost identical to that described in the section entitled "NASA Identification, Binary to Decimal Conversion". This register is more extensive and more loading NAND's are required since the numbers are larger, 15 bits for NASA and 16 bits for RIDL. The loading NAND's (DN units) nearest the BC units are concerned with the NASA word and are enabled by N from the Mode Recognizer only during the NASA interval. Those NAND's directly under the NASA loading NAND's are concerned with RIDL and are enabled only during RIDL interval by R from the Mode Recognizer. An examination of the table on Figure 18, which describes various inputs to these loading NAND's, plus an examination of the Master Timer waveforms will verify that the register is loaded with 1's complement of the NASA or RIDL word in correct bit order. Conversion to 2's complement and final conversion to decimal form is accomplished in the same manner as described for the NASA identification number.

Differences between the two units should be noted. The start pulse A is delayed from G and since this function already has been performed in the NASA identification binary counter and control logic, A is simply wired into this unit. The last stage in the binary counter chain, BC 11-6, is used while the 16-bit RIDL word is processed, but it must be in effect eliminated while the 15-bit NASA word is processed. This is accomplished by always setting this stage to *one* at the proper time, using channel 11 strobe applied to DN 12-31. The count source, MV 16-6, is run at 500 kc as opposed to 100 kc in the identification case. The higher rate is necessary in this case since the number is longer and requires more processing time; in the identification case, a low speed decade on the commercial counter is used, and 100 kc is the top repetition rate allowable. Logic block DM 25-28 must be set to 0.7 μsec in order to conform to the 500 kc input. Logic block DM 18-31 fires when the Mode Recognizer indicates that the satellite signal has changed to the NASA mode; the 200 μsec generated pulse is used to set 0 on the decade counter which compiles the RIDL word count.


BC 2
BC 5
INI27A
DN 3
DN 4
DN 6
DN 7
DM 18 200 μsec
DI 22
DI 17
C 5-6 RIDL WORD
COUNT RESET
C 5-6 (PANEL)
(II, 10-18)
(I, 15-10) Fig. 17
(II, 10-8)
(I, 17-11)
(I, 21-25) Fig. 17
(II, 17-27) Fig. 16

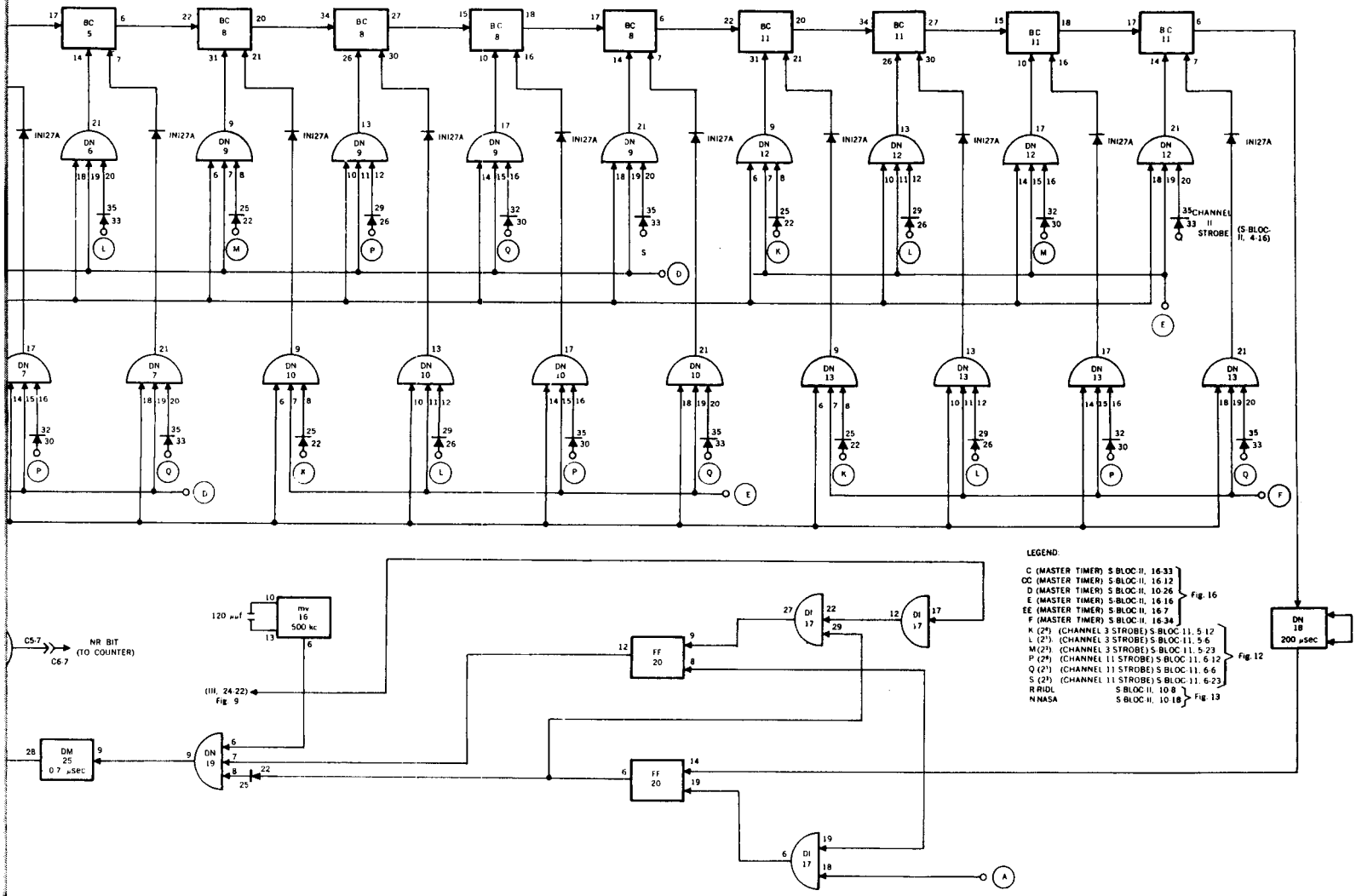


Figure 18–NASA and RIDL register (binary counter) and control logic, S-BLOC-1

RIDL Word Count

The RIDL words are numbered 1 to 64, this number is printed alongside the RIDL word by the commercial printer. To accomplish this, two commercial decades (NOTE 1) are set to zero at the end of the RIDL interval and remain at zero all during the NASA interval. Starting at the beginning of the RIDL interval these two decades are furnished one count per word by the logic shown at top left of Figure 17. Logic block DI 17-23 is an inverter, DI 17-16 is a NAND circuit gated on only during the RIDL interval by input R from the Mode Recognizer. The signal G from the Master Timer occurs only once per word and is used as a word count pulse to the decades.

The reset pulse generated is by the logic at extreme left of Figure 18. Logic block DM 18-31 fires when R from the Model Recognizer goes positive (at beginning of NASA interval). The 200 μsec pulse is inverted by DI 22-16 and is applied to the RESET input of the decades.

NOTE 1: These two commercial decade counters are located in the decimal printer. In order to drive these two counters, special circuitry was added in the printer. A detailed description of this circuitry is given in the RIDL Word Count paragraph in the section devoted to the Commercial Counter Modifications.

SECTION 3

FUNCTIONAL DESCRIPTION OF SUI LOGIC

GENERAL FUNCTIONAL DESCRIPTION

In order to better understand the primary functions of the SUI logic it will be necessary to refer to the SUI waveform charts (Figures 4 and 5) and to the general block diagram (Figure 6).

Decommutation and Detection of Frame Syncronization

The DECOMMUTATOR performs four primary functions. The first is frame synchronization. The second is the separation of each channel, providing 16 individual outputs where each output will give the detected burst of a specific channel within every frame. The third function is that of providing a continuously detected envelope of the inner signal. The fourth function is automatic gain control of the raw signal before it is given to the Comb-Filter so that the Comb-Filter will see a constant amplitude signal.

Conversion of the Digitized Frequency to Binary Form

The COMB-FILTER contains eight filters, each one tuned to one of the eight discrete frequencies (see page 2). A detected frequency, representing a number between 0 and 7, is shaped and then operated on by a matrix which provides a 3-bit number. Buffer stages between the COMB-FILTER and other parts of the equipment are incorporated since the COMB-FILTER circuits operate at different voltage levels than do those in the rest of the equipment.

Description of the Strobe Generator

The STROBE GENERATOR generates 10-μsec pulses that are delayed 5 msec from the beginning of the burst for each of the digital channels (except channel 1). The inputs to the STROBE GENERATOR are the individual channel outputs from the Decommutator. The STROBE GENERATOR provides a means for selecting a particular channel and strobing the outputs of the Comb-Filter for this particular channel to determine the states of the three bits representing the information within that channel.

Detection of Barker Code

The 11-bit Barker code is recognized by the BARKER RECOGNIZER whose output then initiates in the Master Timer the beginning of a count of 21 frames. During this Barker recognition and the 21 frame delay, no word information will be present. After the 21 frames are counted, a NAND matrix opens for a count-by-seven counter which provides four cycle of seven frame counts. This counter and its matrix gates binary word information from the Comb-Filter to the binary registers, initiates register readouts to the Commercial Decimal Counters, provides print commands to the Commercial Printer, and resets the Commercial Decimal Counters.

Loading the Register

There is an 18-bit register (the SUI WORD REGISTER) for the SUI word and a 3-bit register (the SUI IDENTIFICATION REGISTER) for identification. During each gate pulse from the Master Timer, the complement of the 2^0 bit (in the Serial Mode) or of the 2^2, 2^1, and 2^0 bits (in the Parallel Mode) as presented by the Comb-Filter are loaded into the SUI WORD REGISTER and the SUI IDENTIFICATION REGISTER by way of the loading NAND's. Six frames are required to load the SUI WORD REGISTER and one frame to load the SUI.IDENTIFICATION REGISTER. The least significant bit is loaded into the register first.

Conversion of Word from Binary to Decimal; Display; and Printout

The word as collected in the register is in binary form; for quick interpretation it is necessary that it be converted to decimal form, displayed, and printed. This conversion is accomplished by supplying one count to the register (the register is a binary counter), converting 1's complement to 2's complement, and then supplying counts to the binary counter until there is an output from the last stage, which immediately gates off counts to the input. The number of counts required to generate an output from the last stage is equal to the original number–that is, before complementing. The input counts are also supplied to a commercial decimal counter and this counter is therefore loaded with the correct number in decimal form. At a time selected by the Master Timer, this number is printed and the decimal counter is set to zero in preparation for a repeat of the cycle.

The SUI WORD CONTROL LOGIC controls the binary counter. After the SUI Word Register is loaded, a start pulse from the Master Timer is provided to the SUI WORD CONTROL LOGIC which first provides one count pulse to the SUI Word Register and then gates a 500 kc square wave signal into this register. The 500 kc signal continues to run into this binary register until the register is cleared. When the register is cleared, the SUI WORD CONTROL LOGIC will lock out the 500 kc signal. While this 500 kc signal is being gated into the SUI Word Register, the signal is being counted by the Commercial Decimal Counter. The number counted during this readout of the SUI Word Register will then be displayed as the SUI word.

With this information now stored in the decimal counter a print command from the Master Timer, some time later, is provided to the SUI Commercial Printer which in turn prints the displayed word and its identification. The Commercial Counters are reset after one frame time following the print command. This print command is generated in the Master Timer.

DETAILED FUNCTIONAL DESCRIPTION OF THE LOGIC SUBUNITS

For purposes of explanation of logic, consider that the TEST FAST-TEST SLOW OPERATE switch is in the OPERATE position. It is advised that throughout these explanations reference be made to the SUI waveforms, Figures 4 and 5.

Decommutator

The DECOMMUTATOR is explained in Reference 2.

Comb-Filter

The COMB-FILTER is explained in Reference 3.

Buffer Stage

The COMB-FILTER BUFFER STAGE is used to work the Comb-Filter into the Arithmetic Unit because of the heavy loads that the Comb-Filter is required to drive. The COMB-FILTER BUFFER STAGE is shown in Figure 19.

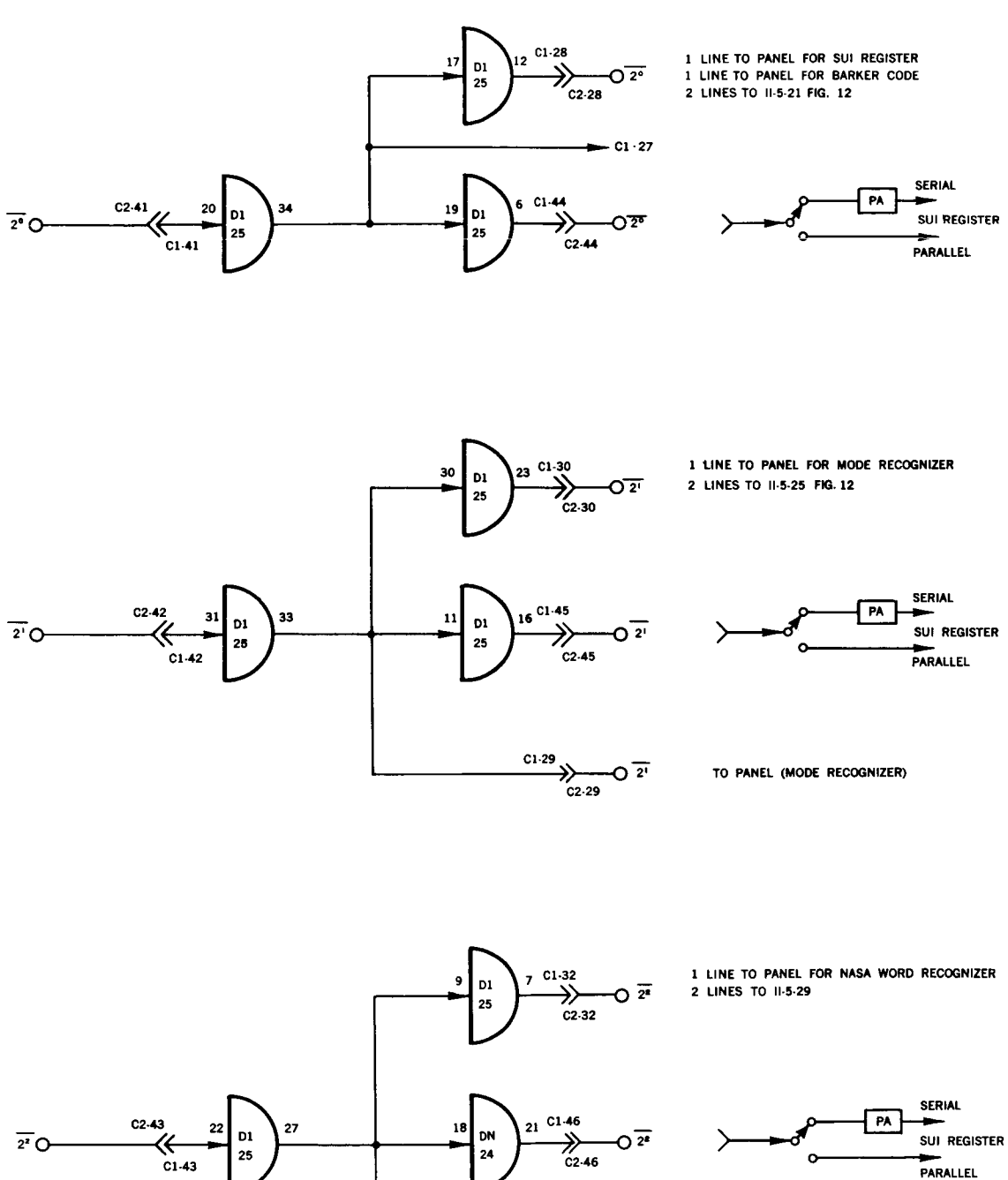


Figure 19–Comb-Filter Buffer Stage, S-BLOC-II

Strobe Generator

Refer to Figures 4, 5, and 20. The detected envelope from the Decommutator is fed to DI 8-34 which functions as an inverter. This inverted waveform is then supplied to DM 7-31, a monostable multivibrator set to generate a 5-msec pulse. This output is then inverted and fed to DM 7-28 which has been set to generate a 10-μsec pulse. Thus, at the output of DI 8-27, an inverter, there will be a train of negative-going 10-μsec pulses occurring in the middle of every burst time, approximately 5 msec after the beginning of each burst. These pulses are applied to eight inverting NAND gates which have as gating inputs the separated envelopes for channels 0, 2, 3, 4, 5, 6, 7, and 11. The logic block DI 3-34 has as an output a positive-going 10-μsec pulse occurring only during channel 0 time and 5 msec after the beginning of the channel 0 burst. The same is true for the other seven channels; DI 3-33 will have a 10-μsec pulse output during channel 1 time, and so on for the other channels. All strobes are fed through inverters in parallel in order to split a large load.

The switch SW-1 is used to change the time constant for DM 24-29 to allow a Test Fast-Test Slow mode. In the Test Fast mode, outputs K, L, and M are binary information from the Comb-Filter which has been NAND'ed with channel 3 strobe. The outputs P, Q, and S are binary information NAND'ed with channel 11 strobe.

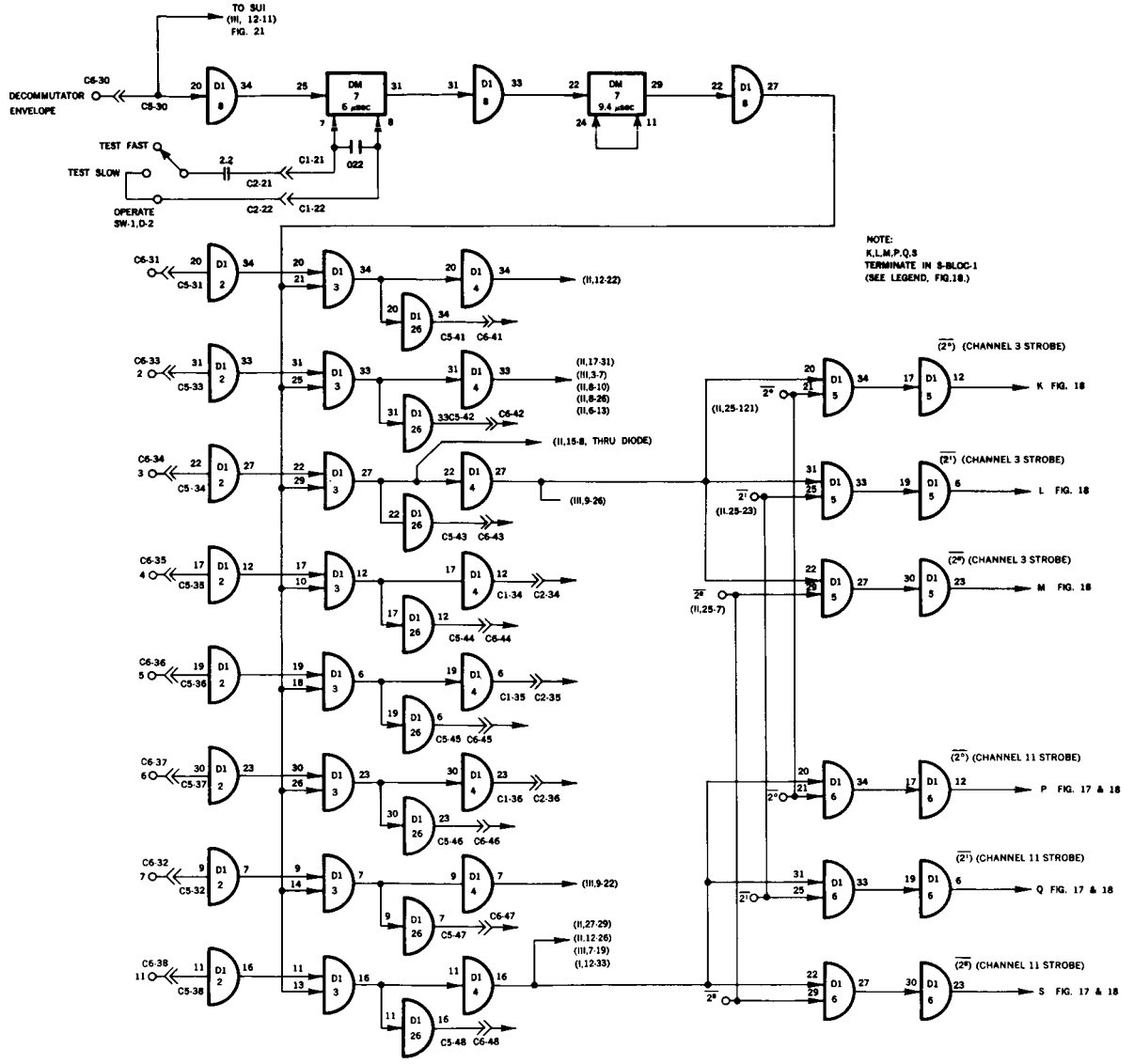


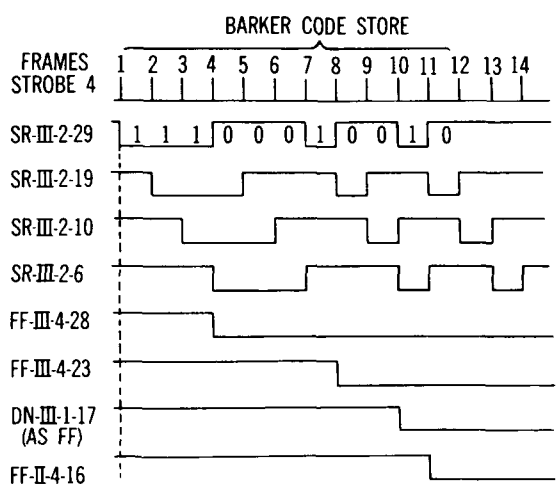
Figure 20–Strobe Generator, S-BLOC-II

Barker Recognition

Recognition of the SUI word cycle by the Barker code takes place in the SUI BARKER RECOGNIZER, see Figure 21. The assertion of the 2^0 bit is gated through DN-III-12-13, and its compliment through DN-III-12-9 by the Decommutator envelope and by FF-III-4-11. (See Figure 22.) Logic block FF-III-4-11 will inhibit these gates during word time, that is, when the signal contains word information. A shift pulse at either channel 4, 5, or 6 strobe time (Note 1) will then store into the first shift register the state presented by the 2^0 bit at that time. The shift pulse will also shift the present state of each shift register to the next shift register. At the beginning of the Barker code all the gates directly associated with the outputs of the shift register are inhibited (Note 2). When the first four bits of the Barker code, 1110, (Note 3) have shifted into the shift register, DN-III-3-21 sets FF-III-4-28 which enables DN-III-3-12. The next four Barker bits, 0010, (Note 4) provide a set pulse to FF-III-4-23 which enables DN-III-1-9. The next two bits, 01, (Note 5) to shift into the register will provide DN-III-1-17 (Note 6) with a set pulse which will enable DN-III-3-17. The last Barker code bit, 0, (Note 7) will provide a set pulse to FF-III-4-16 which indicates to the Master Timer that Barker code recognition has taken place.

Note 1: The strobe used for shifting is dependent upon the setting of the SUI format switch. In Serial, channel 4 strobe is used. In Parallel, the switch selection indicates which strobe is used.

Note 2: The Barker Recognizer waveforms are:



Note 3: At this time the set outputs of the shift registers in Figure 21 will appear in this order: 0111.

Note 4: At this time the set outputs of the shift registers in Figure 21 will appear in this order: 0100.

Note 5: At this time the set outputs of the shift register will appear in this order: 1001.

Note 6: Logic blocks DN-III-1-17 and DN-III-1-21 work together as a dc flip-flop.

Note 7: At this time the set outputs of the shift register will appear in this order: 0100.

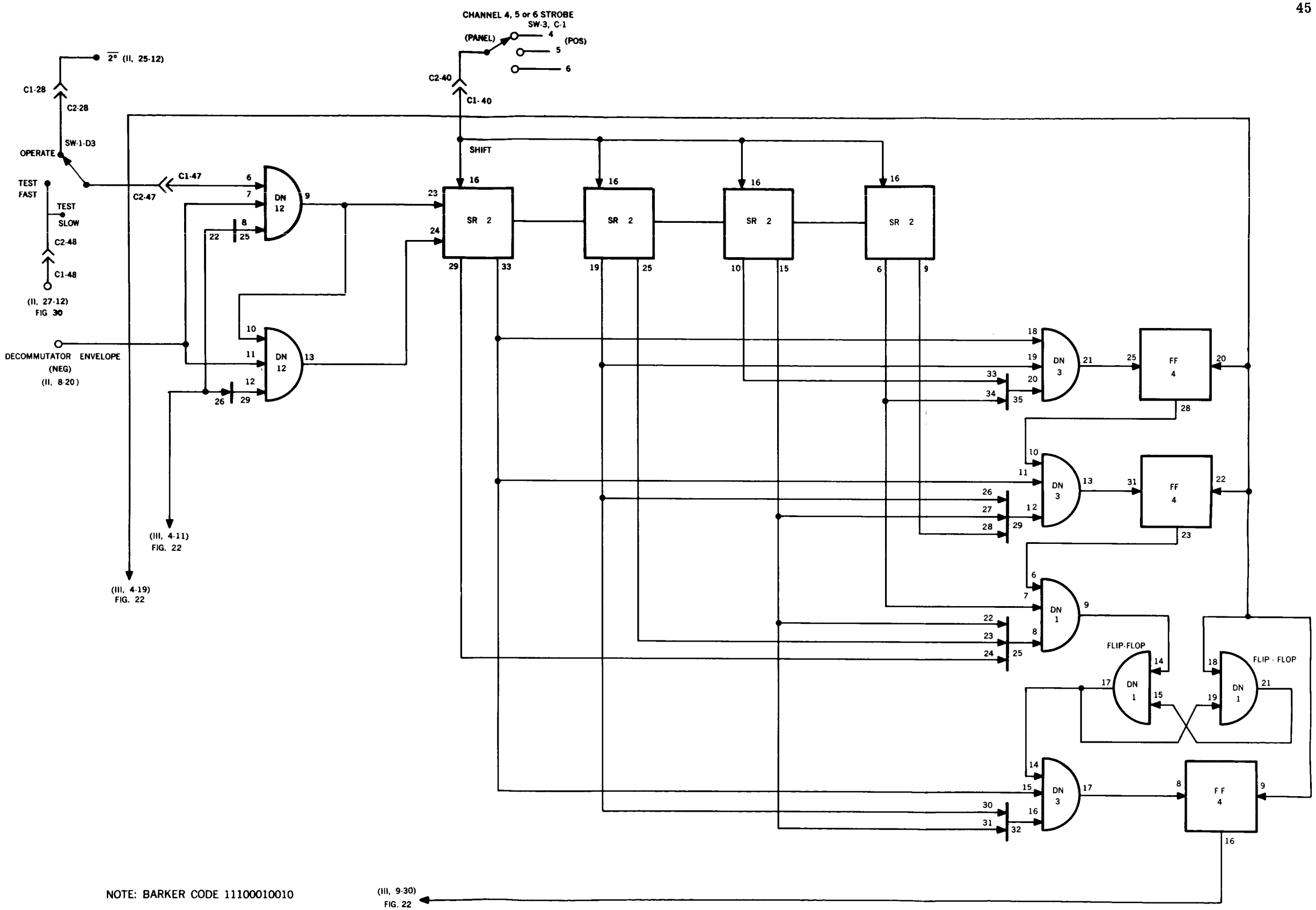


Figure 21—SUI Barker Recognizer, S-BLOC-III

Master Timer

Refer to Figure 22. Upon recognition of the Barker code, the output of the Barker Recognizer will enable DI-III-9-23; thereby gating channel 3 strobe (Note 1) into the MASTER TIMER counter. This counter is not wired as a normal binary counter but counts in a manner exclusively for SUI timing. See Figure 4. Upon receiving 21 counts, the fifth stage of the counter BC-III-11-20 will change state, toggling DM-III-5-29 which, in turn, resets the Barker Recognizer flip-flops and FF-III-4-6. The new state of the Barker Recognizer flip-flops will inhibit the former counter gate, DI-III-9-23. The set output of FF-III-4-11 will inhibit the Barker code gates DN-III-12-9 and DN-III-12-13 and enable the MASTER TIMER DN gates associated with the counter matrix. The reset output of FF-III-4-11 will enable two gates to the input of the counter, DN-III-3-9 and DN-III-7-21 (through the latter DN will still be inhibited by DI-III-8-7 until frame 7).

The counter will then begin to accept channel 2 strobe counts (Note 2). Note that the counter is not reset—it continues to count. The matrix is designed to give four cycles of seven sequential outputs. This is done by advancing a count-by-eight counter (the first three BC's) by one count in each of the four cycles. During the seventh frame, DI-III-8-7 enables DN-III-7-21 thereby allowing the extra count, channel 11 strobe, to return the first three BC's to the initial starting state. Inspection of Figures 4 and 22 will show how the print, reset, start, and identification start pulse are generated from this matrix.

Note 1: Since the Barker Code is given in either channel 4, 5 or 6, the MASTER TIMER counter will begin to count on the next frame.

Note 2: Since the 21 frame count counted channel 3 strobe pulses, the count-by-seven counter will begin to count on the next frame following the 21 counts.

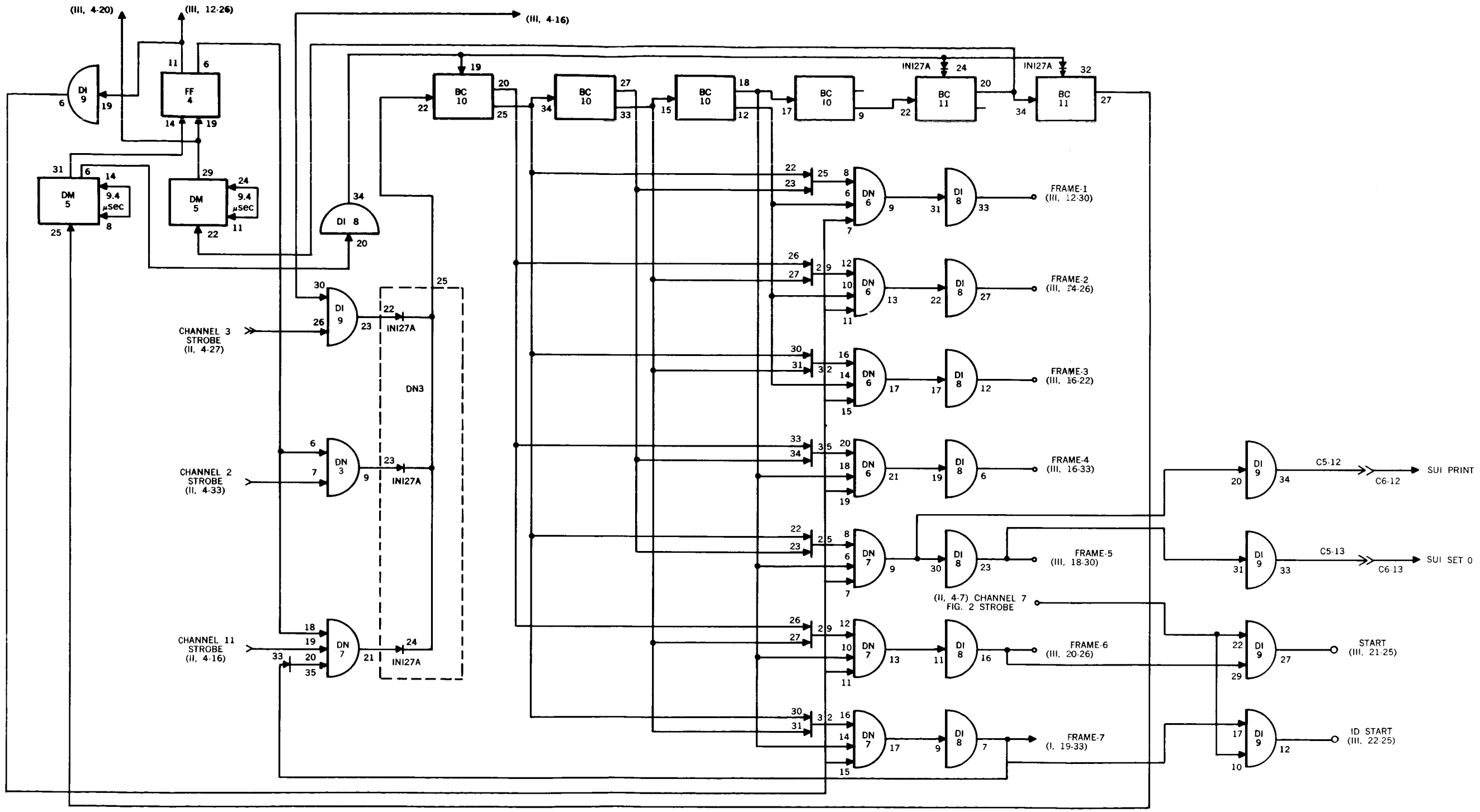


Figure 22—SUI Master Timer, S-BLOC-III

SUI Counter and Control Logic

Refer to Figures 23 and 24. With the Master Timer providing the proper gating sequence, the loading NAND's below the counter BC's gate into the binary counters the compliment of the binary bit presented at the Comb-Filter at the appropriate time. There are two methods by which information is given to the loading NAND's: one for the Serial mode and one for the Parallel mode. The logic for these two methods of loading the register may best be explained by discussing the loading during one frame (involving 3 bits) for each method. Loading throughout the rest of the register will, of course, be analogous to the loading of the first three binary counters.

METHOD ONE—THE SERIAL MODE

Here the 2^0 bit is provided to all the loading NAND's.

The loading NAND's, DN-III-12-17, DN-III-12-21, and DN-III-14-9, will be enabled by frame 1 from the Master Timer. Channel 4 strobe, always present at DN-III-12-14, will then provide an output at DN-III-12-17 if the $\overline{2^0}$ bit at that time is in a *one* state. Thus, the compliment of the 2^0 bit during frame 1 channel 4 is loaded into the first BC, BC-III-11-18. The next channel strobe, channel 5 strobe, is applied to DN-III-12-21 and an output from this NAND gate will be given if the $\overline{2^0}$ bit at that time is in a *one* state. Channel 6 strobe is likewise provided to DN-III-14-9 so that the $\overline{2^0}$ bit will provide a set pulse to BC-III-13-20 if the $\overline{2^0}$ bit was in a *one* state. In this one frame time, three bits of information were loaded into the first three registers.

METHOD TWO—THE PARALLEL MODE

In this mode the selected channel strobe, either 4, 5, or 6, will enable all the NAND's. Again, as was the case for the Serial Mode, frame 1 will enable the first three NAND's. The state of the $\overline{2^0}$ bit will always be present to the first NAND, DN-III-12-17, the state of the $\overline{2^1}$ bit will always be present to the second NAND, DN-III-12-21, and the state of the $\overline{2^2}$ bit will always be present to the third NAND, DN-III-14-9. With this gating then, it can be seen that at channel 4 time the compliment of the 2^0 bit will be loaded into the first binary counter BC-III-11-18. At channel 5 time the compliment of the 2^1 bit will be loaded into BC-III-11-6, and at channel 6 time the compliment of the 2^2 bit will be loaded into BC-III-13-20.

GENERAL

The method of loading the first three BC's, for either of the two methods, is repeated for each successive group of three binary counters in the register each group requiring

separate frame gates from the Master Timer. In like manner, the SUI identification bits (in compliment) are loaded into the identification register. Refer to Figure 23.

With the binary compliment of the SUI word loaded in the word register, a 10-μsec start pulse is provided from the Master Timer to the input of the Control Logic at two points, one an input to a NOR and the other an input to a delay-multivibrator. The input to the NOR, DI-III-25-20, introduces into the binary register one more count. The input to the delay-multivibrator, DM-III-21-25, sets the DM for a 15-μsec delay which then triggers DM-III-21-10. This DM will initiate the register readout. The purpose of this delay is to allow time for the NOR discussed above to have returned to its steady-state zero output. The extra count will then have been stored in the register, and the register will be in a prepared state for the control logic to gate into the register a 500-kc signal.

The delayed pulse from DM-21-10 is applied through DI-25-12 to FF-23-27 throwing this flip-flop to the state which gates on DI-25-6 and DN-24-9. (The function of DM-21-28 will be explained later; at this point, it will suffice to say that it is quiescent and in a state which gates on DI-25-12.) Logic block DN-24-9 is now gated on at pin 7 and has applied at pin 22 a 500 kc square wave from MV-16-6 in S-Bloc-I. If the input at pin 6 of DN-24-9 were eliminated, then the desired end would be achieved–that is, counts would be introduced into the binary counter on signal from the start pulse. However, since the start pulse and 500 kc square wave are not synchronized, the first pulse from DN-24-9 could be a partial pulse of varying width and in some cases would cause a partial, or sliver, output from the multivibrator DM-26-28. The logic performed by DI-25-12, DI-25-6, and FF-23-33 is to eliminate the possibility of this partial first pulse. Flip-flops FF-23-33 will throw to the state gating on DN-24-9 at pin 6 only when (1) FF-23-27 has thrown to the state gating on DI-25-6, and (2) MV-16-6 in S-Bloc-I is in the positive portion of its cycle. Logic block DN-24-9 will now pass the next negative-going pulse from MV-16-6, S-Bloc-I. An analysis of this section shows that a full width first pulse is guaranteed. This 500 kc square wave will then begin to "readout" the binary register. Each "readout" pulse is counted by the commercial counter. When the binary register sets to all zeros, DM-21-28 will be triggered and its output will reset FF-23-27 thereby gating off the 500 kc signal to the register and the commercial counter. The WORD CONTROL LOGIC gates in a 500-kc signal, from MV-I-16-6, and the IDENTIFICATION CONTROL LOGIC gates in a 100-kc signal. The 500-kc signal to the commercial decade counter leaves the WORD CONTROL LOGIC at DN-III-1-13, and the 100-kc signal to the added decade, located in the commercial printer, leaves the IDENTIFICATION CONTROL LOGIC at DM-III-26-29. The circuitry used to drive the identification decade is explained in the section on counter modifications. The maximum SUI word readout requires 524 msec, which allows a sufficient interval between a past readout and the beginning of a new word storage in the binary register. With the SUI word and identification stored in decimal form in the commercial counter and extra decade, a print command is generated (at frame 5 channel 2 time of the next word—see Figure 4) which

will print this word and its identification. The print command is generated in the matrix section of the Master Timer—see Figure 22. Note that the print will occur at the leading edge of the pulse, a negative step voltage.

One frame later, a reset pulse, the inversion of the print command pulse, is provided from the Master Timer and sent to the commercial counter to reset the decades, including the identification decade in the printer. Note that the reset occurs at the trailing edge of the pulse, a negative step voltage. Inspection of the SUI waveforms (Figures 4 and 5) will clarify these print and reset cycles. For an explanation of the circuitry used to drive the printer and the counter reset circuit refer to the section on counter modifications.

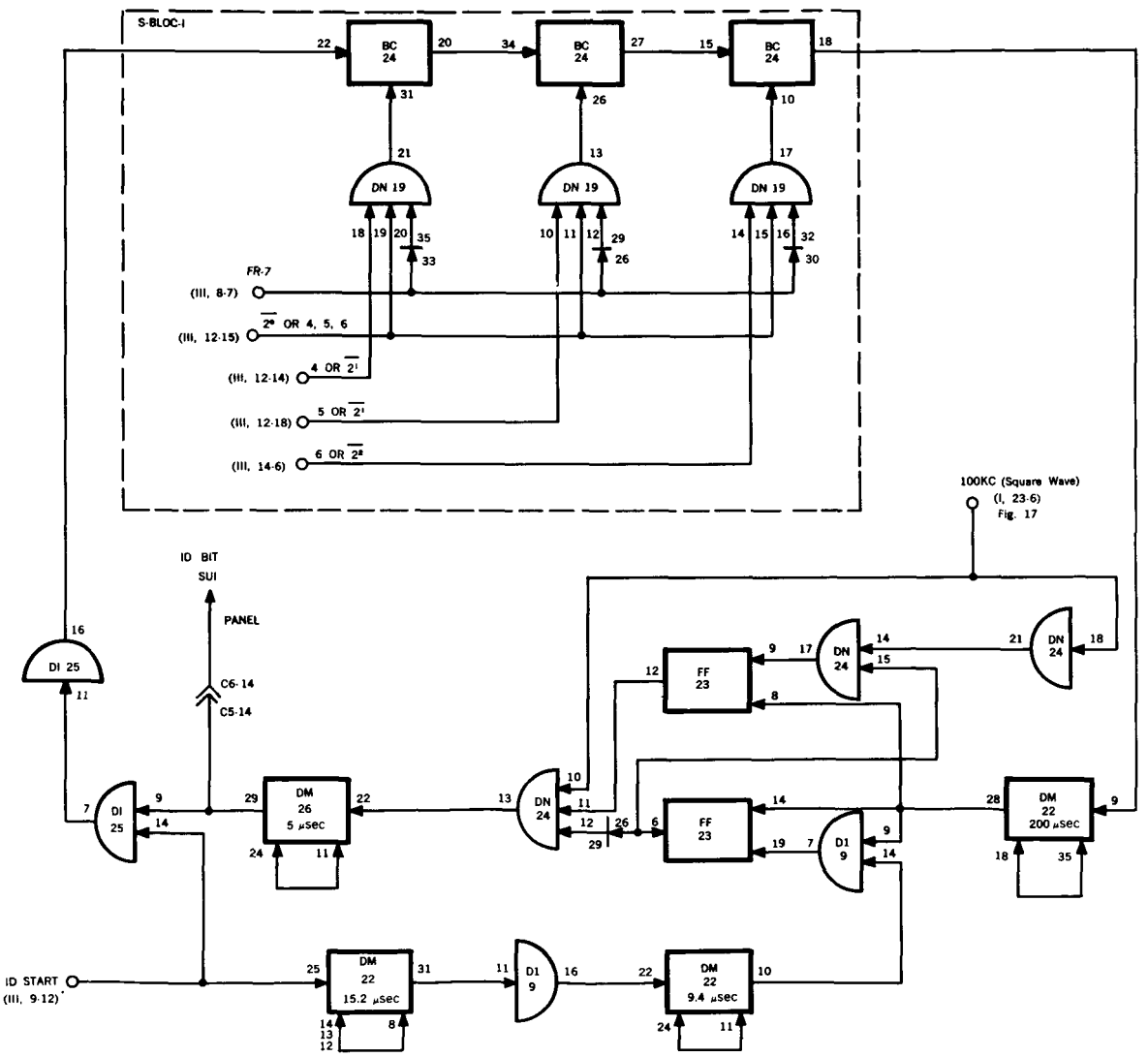
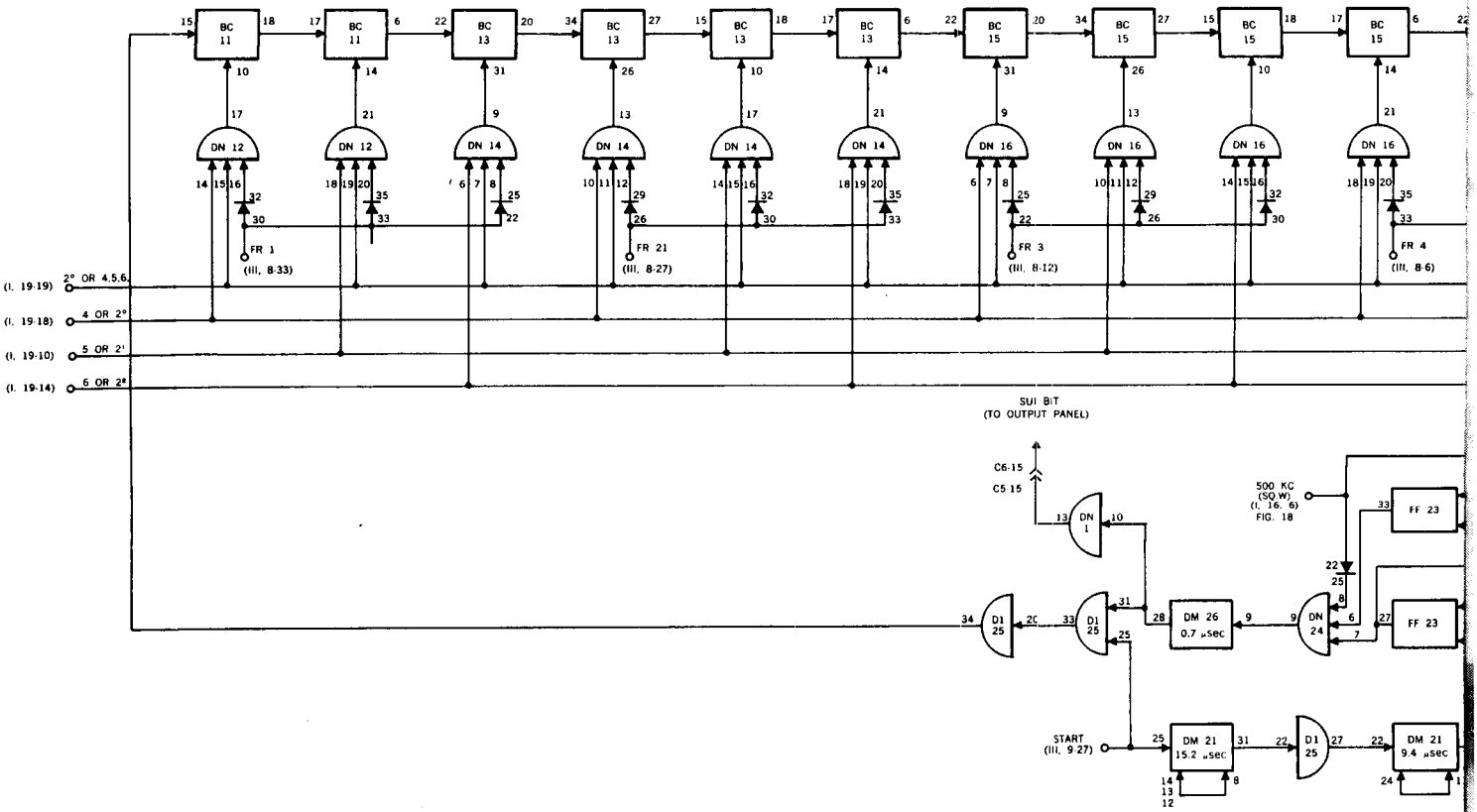


Figure 23—SUI Identification Control, S-BLOC-III and SUI Identification Steering, S-BLOC-I


BC 11
BC 13
BC 15
DN 12
DN 14
DN 16
FR 1
(III, 8-33)
FR 21
(III, 8-27)
FR 3
(III, 8-12)
FR 4
(III, 8-6)
(I, 19-19) 2° OR 4,5,6
(I, 19-18) 4 OR 2°
(I, 19-10) 5 OR 2¹
(I, 19-14) 6 OR 2⁸
SUI BIT
(TO OUTPUT PANEL)
C6-15
C5-15
DN 1
500 KC
(SQ.W)
(I, 16, 6)
FIG. 18
FF 23
DM 26
0.7 μsec
DN 24
D1 25
START
(III, 9-27)
DM 21
15.2 μsec
DM 21
9.4 μsec

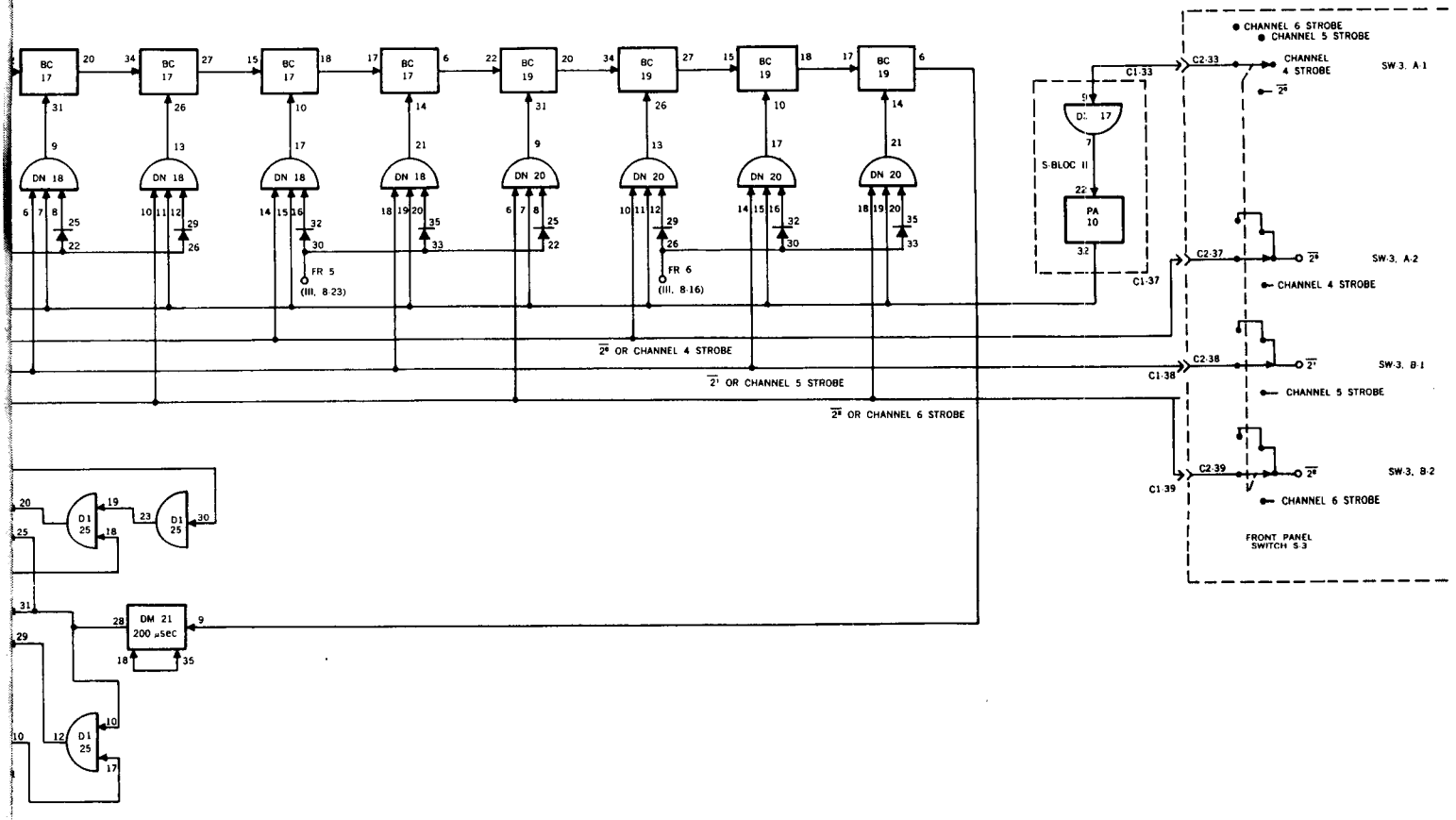


Figure 24—SUI Register and Control Logic, S-BLOC-III

SECTION 4

COMMERCIAL COUNTER MODIFICATIONS

GENERAL

The decimal counter is provided with two switches on the rear panel which will switch the counter from normal counter operation to data reduction operation, the switching brings into use the added modified circuit in the counter. The schematic and layout of this modified circuit can be seen in Figures 25, 26, and 27. The circuit serves three purposes: (1) to provide a print command pulse, (2) to provide a counter reset pulse, and (3) to provide a separate count voltage to the last decade. All three inputs to the circuit are generated in the arithmetic section. Each circuit will be described separately.

The NASA and RIDL counter modification and the SUI counter modification are shown in Figure 28; the difference between these modifications can be determined from this figure.

The details of the Reset and Identification Circuits are shown in Figure 29.

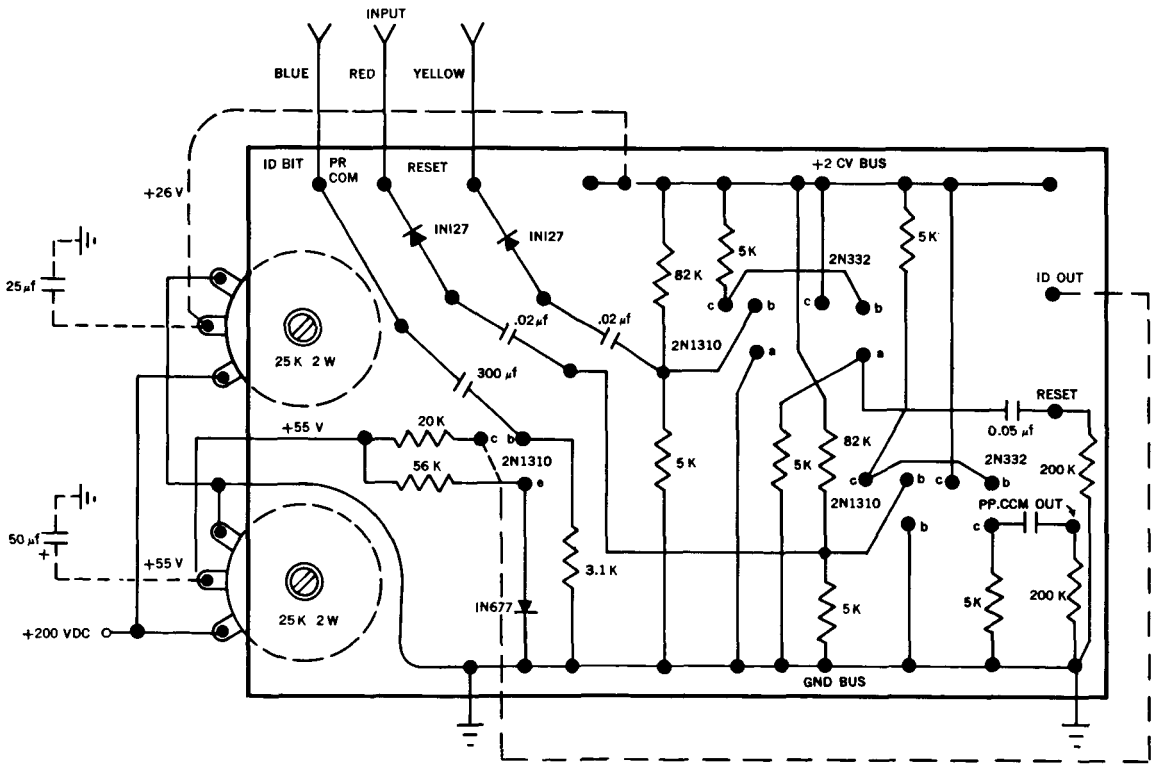


Figure 25—Commercial counter modification board layout

COMMERCIAL PRINTER

Print Command

The print-command input from the arithmetic unit is a negative-going 6-volt pulse. The repetition rate of this pulse should not be less than 200 msec. Normally T_1 is biased "on". A negative step voltage at the input will be coupled through the input capacitor and drive T_1 "off", allowing the output to take a 25-volt positive step. The base voltage will then decay toward the normal bias voltage with a time constant given by C_1 and the parallel impedance of 5.1 kilo-ohms, 82 kilo-ohms, and the equivalent resistance of the transistor as seen from the base. When the base voltage reaches ground level, the transistor will begin to turn on, returning the output to ground. The transistor T_2 is employed as an emitter-follower, capacitively coupled to the output of the print-command circuit.

The output of this circuit is then sent to the printer by way of pin L of the counter output connector (through the added switch).

Reset

The input and output requirements for the reset circuit are precisely the same as those for the print-command circuit. The reset circuit is, therefore, the same as the print-command circuit. The output is wired to pin 1 of V405 (through the added switch) in the counter which is the grid of the reset thyratron. The 26-volt step will drive the tube into firing, reseting the decades.

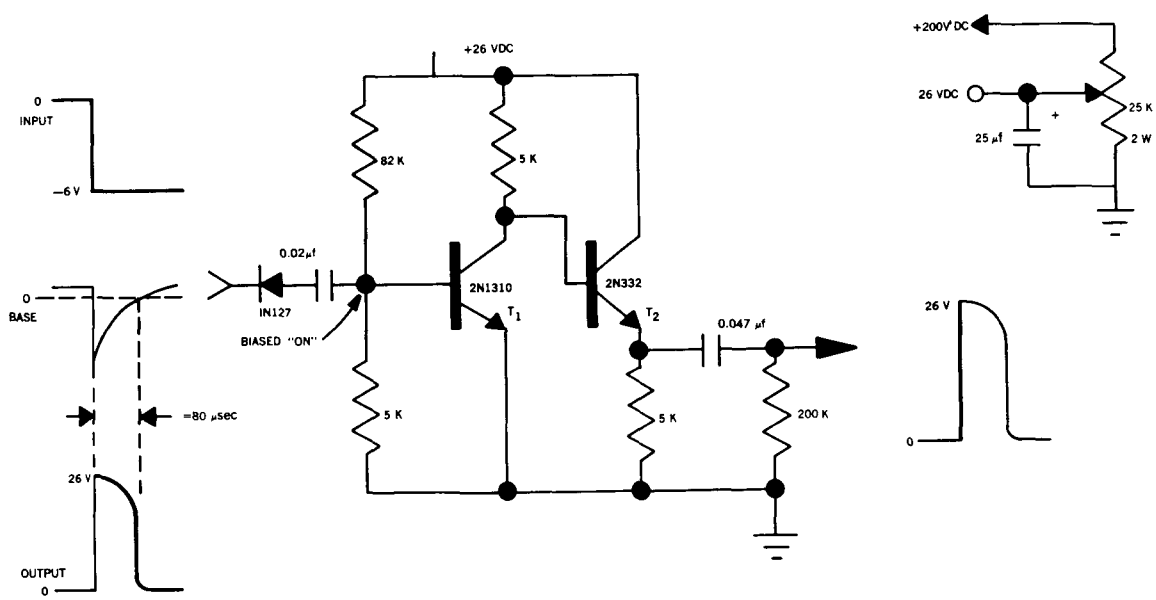


Figure 26–Reset and print-command circuit is (identical circuits). The first circuit resets the output to pin 1 of V405. The second circuit gives the pin command output to pin L of the counter-printer connection.

Identification Bit Circuit

The IDENTIFICATION BIT CIRCUIT is a dc amplifier which provides to the input of the last (most significant) decade of the counter a negative-going 50-volt step voltage required to trigger the AC-4G decade for the identification count. The input to the dc amplifier is a 100-kc square wave. A count will be made when the input to the dc amplifier takes a positive-going 6-volt step. The transistor T_3 is normally biased "off" by the voltage drop across the 1N677 diode emitter. A positive-going step voltage at the input will then turn T_3 "on", providing the required 50-volt negative-going step to trigger the decade.

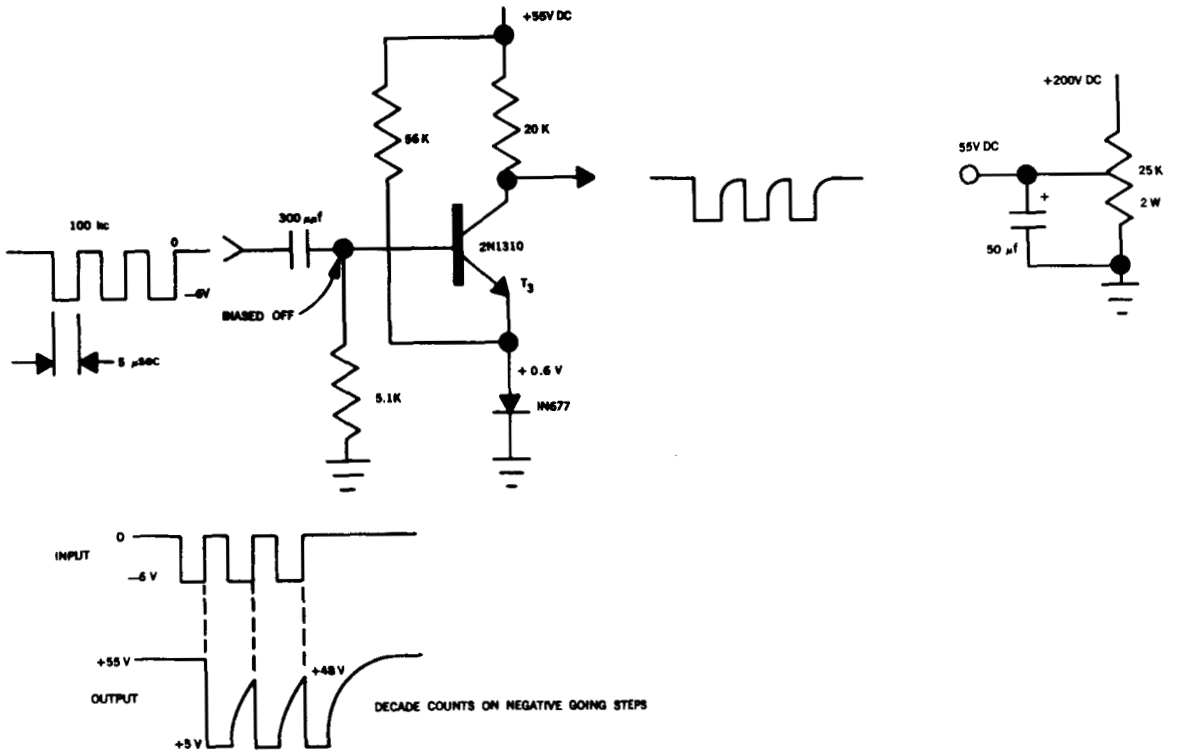


Figure 27—Identification bit circuit. The identification bit output goes into pin 3 of the last decade counter.

RIDL Word Count

Refer to Figure 29. In the NASA and RIDL printer there are two AC-4G decades used for the RIDL word count. Two circuits are used, one to drive the first decade and one to reset these decades. The circuit used to trigger the first decade is a duplicate of the dc amplifier that was added in the commercial counter.

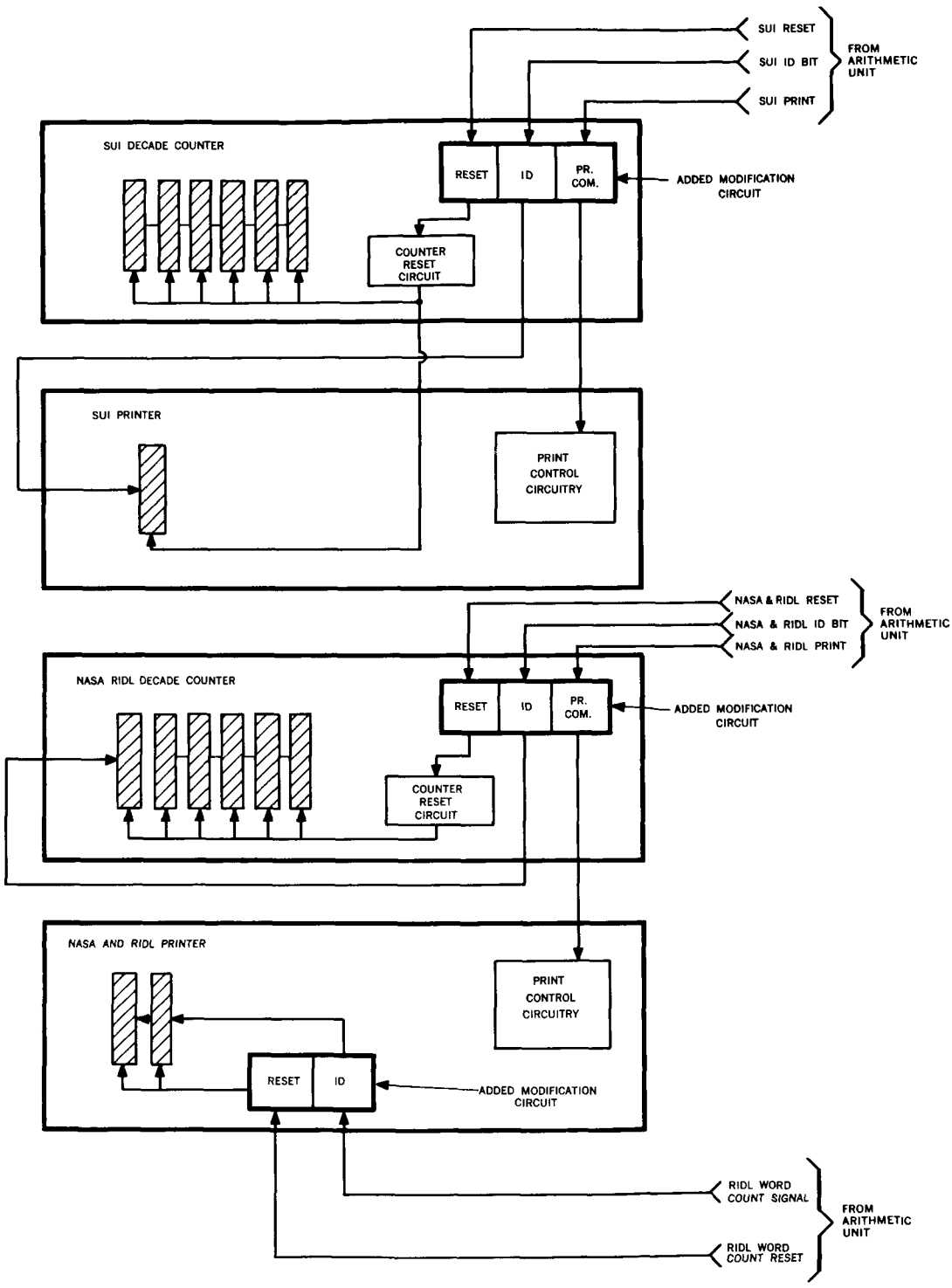


Figure 28–Flow chart for the modification circuits incorporated in the decimal counters and printers. The shaded blocks are the decade counters.

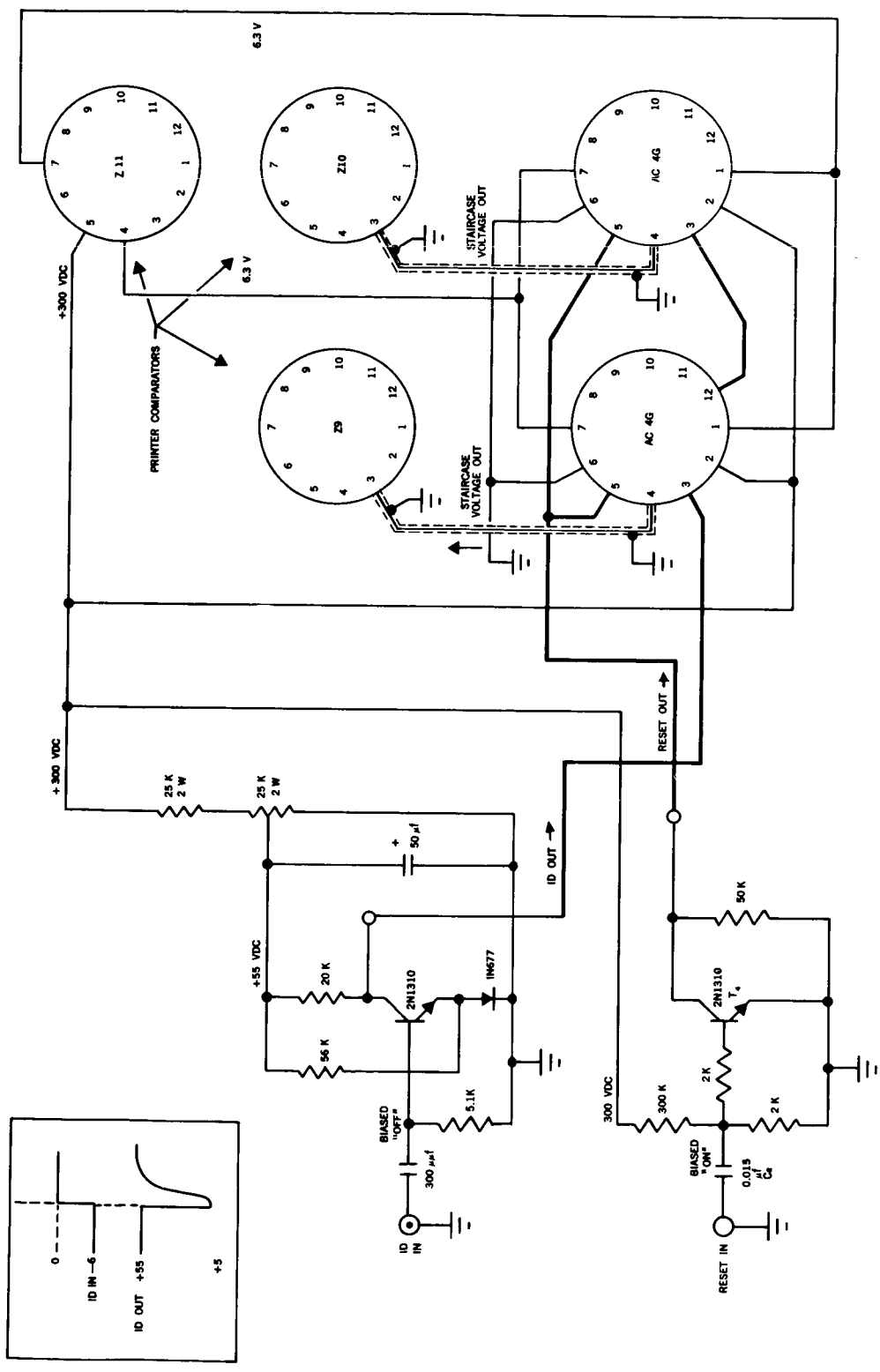


Figure 29–RIDL word count circuit and decade connections (located in the NASA and RIDL printer)

Transistor T_4 in the reset circuit is normally biased "on". In this state, the output will be at ground. A negative-going step voltage at the input will turn the transistor off. The impedance seen by pin 5 of each decade will then be very nearly 50 K since the off impedance from collector to emitter is very high. If a high impedance, on the order of several kilo-ohms, is seen from pin 5 to ground, the decade will reset. Therefore, 50 K provides positive resetting. The transistor will remain off for a time governed by the RC time constant given by C_2 and about 1 K (about 80 μsec).

SECTION 5
EXPLORER XII SIMULATOR

FUNCTIONAL DESCRIPTION OF SIMULATOR LOGIC

Refer to Figure 30. For the purpose of checking out the Explorer XII test stand data reduction equipment, a simulator is incorporated in the equipment to simulate the detected receiver signal and to simulate the envelope of the bursts and blanks. Two repetition rates are available: one equal to the real signal, the other faster by a factor of 100. This fast mode allows practical trouble-shooting of the arithmetic unit using the oscilloscope. At the fast rate, only the simulated envelope of the bursts and blanks is available. The Test Fast-Test Slow-Operate switch (switch 1) controls the repetition rate of this simulator. In normal operation, the simulator is not used. For the NASA and RIDL experiments there are three kinds of simulation; the positioning of the Operate-NASA Test-RIDL Test switch determines what kind of simulation is being used. In the Operate Position of this switch, the NASA experiment and the RIDL experiment will time share for continuous cycles of 16 NASA words and 32 RIDL words. In the NASA Test Position, only the NASA experiment will cycle continuously. In the RIDL Test Position, only the RIDL experiment will cycle continuously.

Through binary counting and gating, principal waveforms are simulated in order that each experiment (SUI, NASA, and RIDL) will be provided with recognition. Once recognition takes place each experiment's Master Timer will then cycle through its experiment.

DETAILED DESCRIPTION OF SIMULATOR LOGIC

The source of timing is a free-running multivibrator, MV-II-18-9, which will be the channel rate. In the Test Slow mode, its repetition rate is 20 msec; this gives a square wave which changes state every 10 msec. In the Test Fast mode, the repetition rate is about 0.2 msec. (The rate here is not critical since its purpose is only for oscilloscope monitoring of the arithmetic unit in checkouts.) In spection of this multivibrator in Figure 30 will show the capacitive changes required to give these two repetition rates. This multivibrator drives a scale of 16 binary counters whose last stage triggers a one-shot multivibrator, DM-II-7-28. This delay multivibrator is given a pulse duration of 15 msec in the Test Slow mode and about 0.15 msec in the Test Fast mode. The output of this delay multivibrator is NOR'ed with the output of MV-II-18-9 to provide a simulated envelope of the synchronizing burst and its following 15 bursts and blanks. This envelope is applied directly to the decoder in the Test Fast mode by SW-1 and B-2. In the Test Slow mode, this envelope gates in and out a sine wave oscillator, board II-20-20 (Figure 31), simulating the detected receiver signal. The frequency of this board is variable from 5 to 15 kc and is controlled by the front panel simulator frequency controls COARSE and FINE. In order to generate the various recognition waveforms, a binary scale of the 256 counter is triggered by each synchronizing pulse. The last binary counter, BC-II-22-6, will change state every 128 frames, changing the states of R and N, the Mode Recognition Signals for NASA and RIDL, at these times (to be employed only when the Test Fast-Test Slow-Operate switch is in the Operate position). The fourth binary counter, BC-II-21-6, provides the simulated 2^2 and $\overline{2^2}$ bits for NASA word recognition. It will change state every eight frames. Gating from BC-II-21-20 and BC-II-21-27 provides an output at DI-II-27-33 every four frames for RIDL word recognition. The Barker code is generated at DI-II-27-12 every 64 frames through gating from this binary counter.

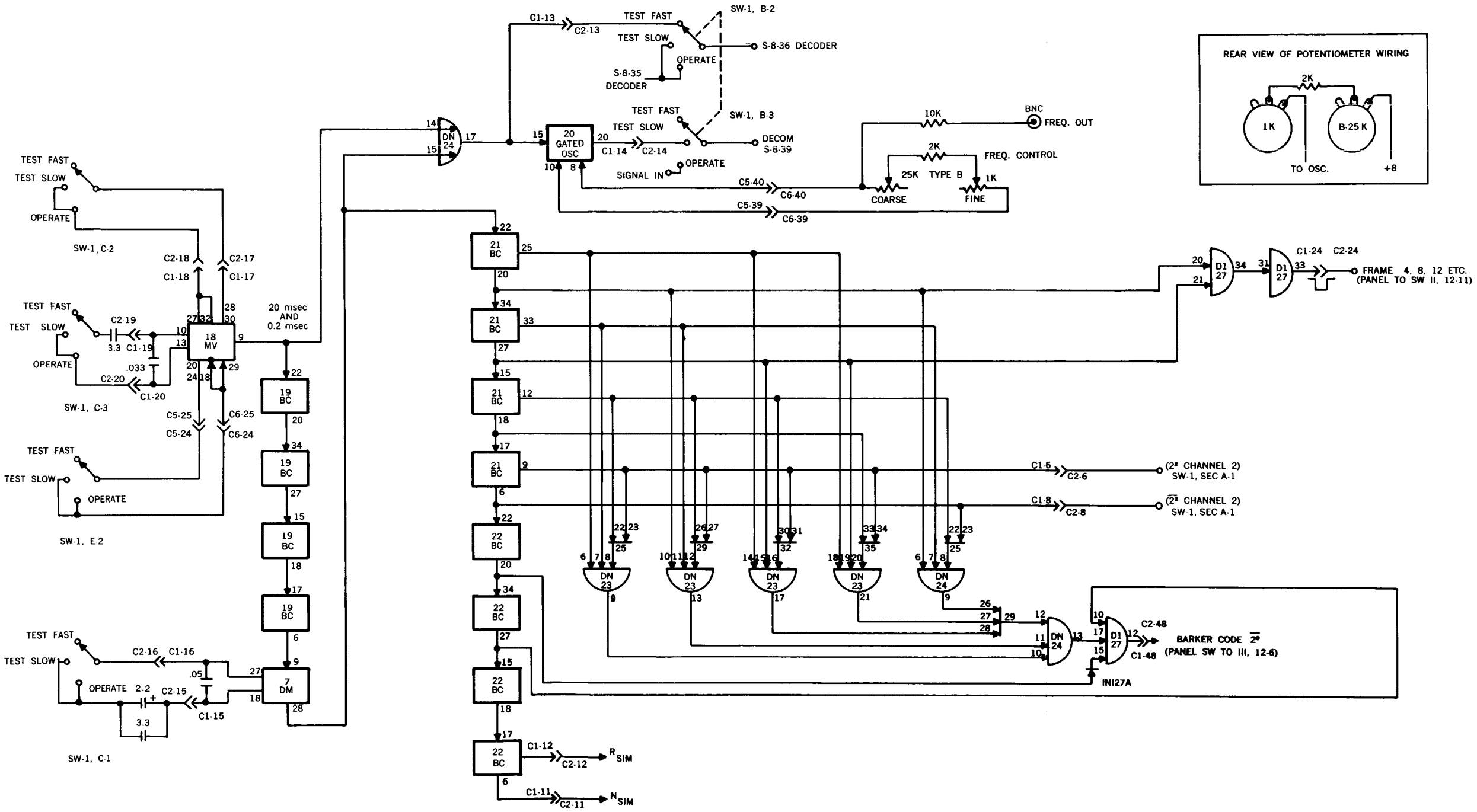


Figure 30—Explorer XII Simulator, S-BLOC-II

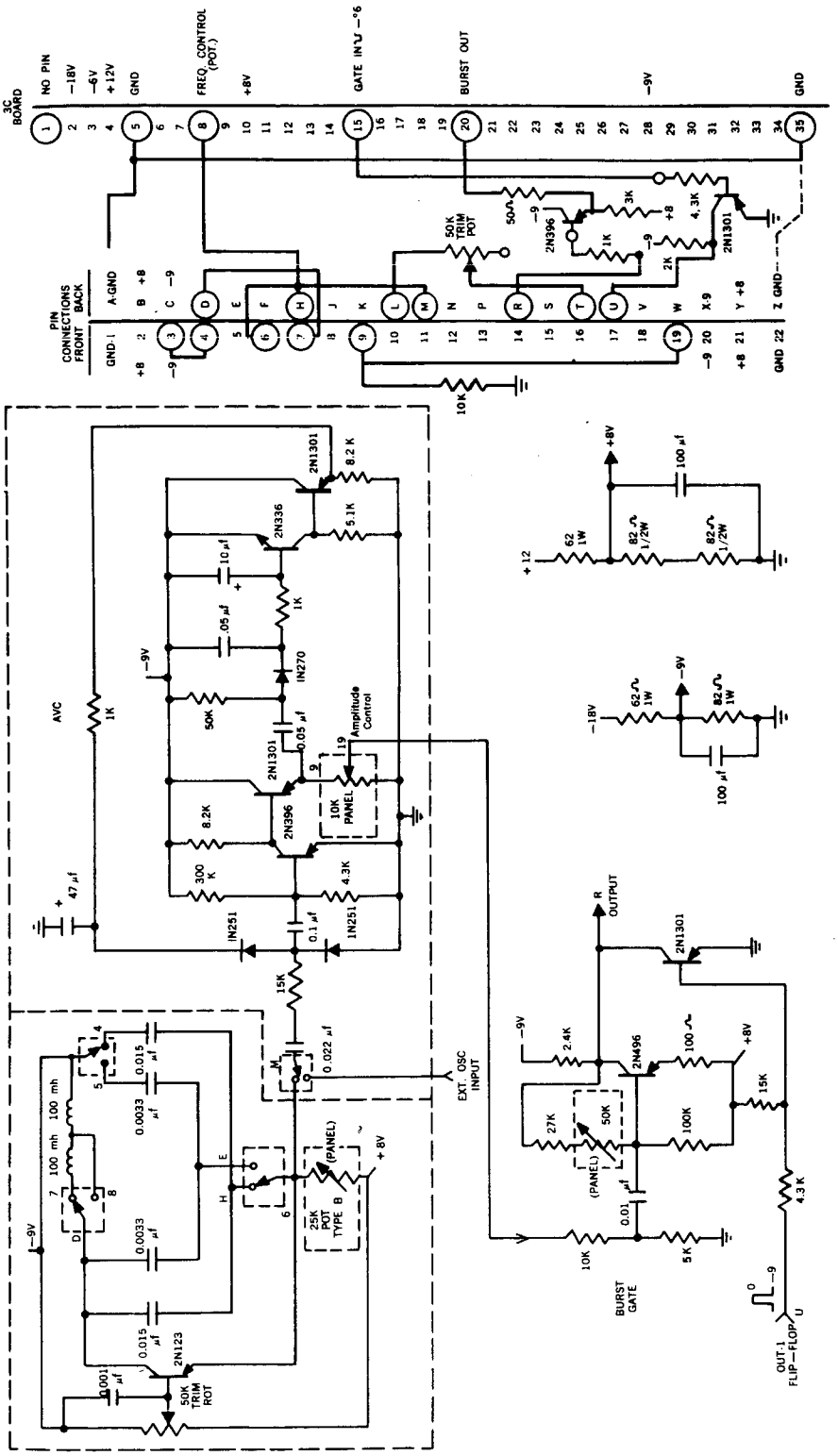


Figure 31—Simulator oscillator board

SECTION 6
SWITCHES

SWITCH 1

The switch 1 interconnectors are shown in Figure 32. Switch SW-1, a 3-position, 13-pole switch, is provided to allow the equipment to be changed from OPERATE condition to two test conditions: TEST SLOW and TEST FAST. The TEST SLOW position is used for a pre-operation checkout described in the section on operating procedures. The TEST FAST position speeds up operation by a factor of 100 and is used only while trouble-shooting of the equipment is taking place. The following discussion describes briefly the function of each portion of SW-1.

The switches SW-1, Sec A-1 and SW-1, Sec A-2 are on the NASA Word Recognizer. These two sections connect the logic to that position of the simulator which simulates the action of the 2^2 and $\overline{2^2}$ bits at channel 2 time.

Switches SW-1, Sec A-3 and SW-1, Sec B-1 are connected to the Mode Recognizer (Figure 13). In this case, the function of SW-1 is to connect the Mode Recognizer logic to that portion of the simulator which simulates the action of 2^1 and $\overline{2^1}$ at channel 2 time.

Switch SW-1, Sec B-2 is on the Simulator (Figure 30). In TEST FAST position, this section of the switch breaks the logic section of the Decommutator from the input section (AGC and detector and shaper).

Time constants in the input section of the Decommutator are too slow to respond at high-speed operation in the TEST FAST mode. A Square wave from the simulator is fed directly into the logic portion of the Decommutator. In TEST SLOW and OPERATE positions, the broken connection in the Decommutator is closed by SW-1, B-2.

Switch SW-1, Sec B-3 is on the Simulator (Figure 30). In OPERATE position, the Decommutator receives SIGNAL IN from the satellite; in TEST SLOW, a simulated burst-blank signal from the Simulator Gated Oscillator is supplied to the Decommutator. The TEST FAST position is open since, in this position, the input section of the Decommutator is bypassed as described in the preceding paragraph.

Switch SW-1, Sec C-1 (Figure 30) changes the pulse width generated by the monostable multivibrator DM-7-28. This is accomplished by selecting different values of time-constant-determining capacitors as shown in the diagram.

Switches SW-1, Sec C-2, SW-1, Sec C-3, and SW-1, Sec E-2 change the repetition rate of a stable multivibrator MV-18-9.

Switch SW-1, Sec D-1 is located on the RIDL Word Recognizer (Figure 15). In the two test positions, this switch connects DN-12-13 to that portion of the Simulator which simulates the action of the 2^2 bit channels 3 and 11, during the RIDL mode.

Switch SW-1, Sec E-2 is on the Strobe Generator (Figures 12 and 20). This portion of SW-1 changes the time constant of DM-7-31 so that when the simulator is operating in the TEST FAST condition, strobe pulses will be generated to fall in the proper position in the speeded up signal.

Switch SW-1, Sec D-3 is located on the Barker Recognizer (Figure 21). In the two test positions, this section of SW-1 connects the Barker Recognizer logic with a simulated Barker code generated in the Simulator.

SWITCHES 2 AND 3

Figures 33 and 34 show the pin connections for the other two wafer switches and indicate the function with which each section is concerned. The manner in which these switches are used is straightforward and may be easily understood by inspection of their connections as shown on the individual logic diagrams of the system.

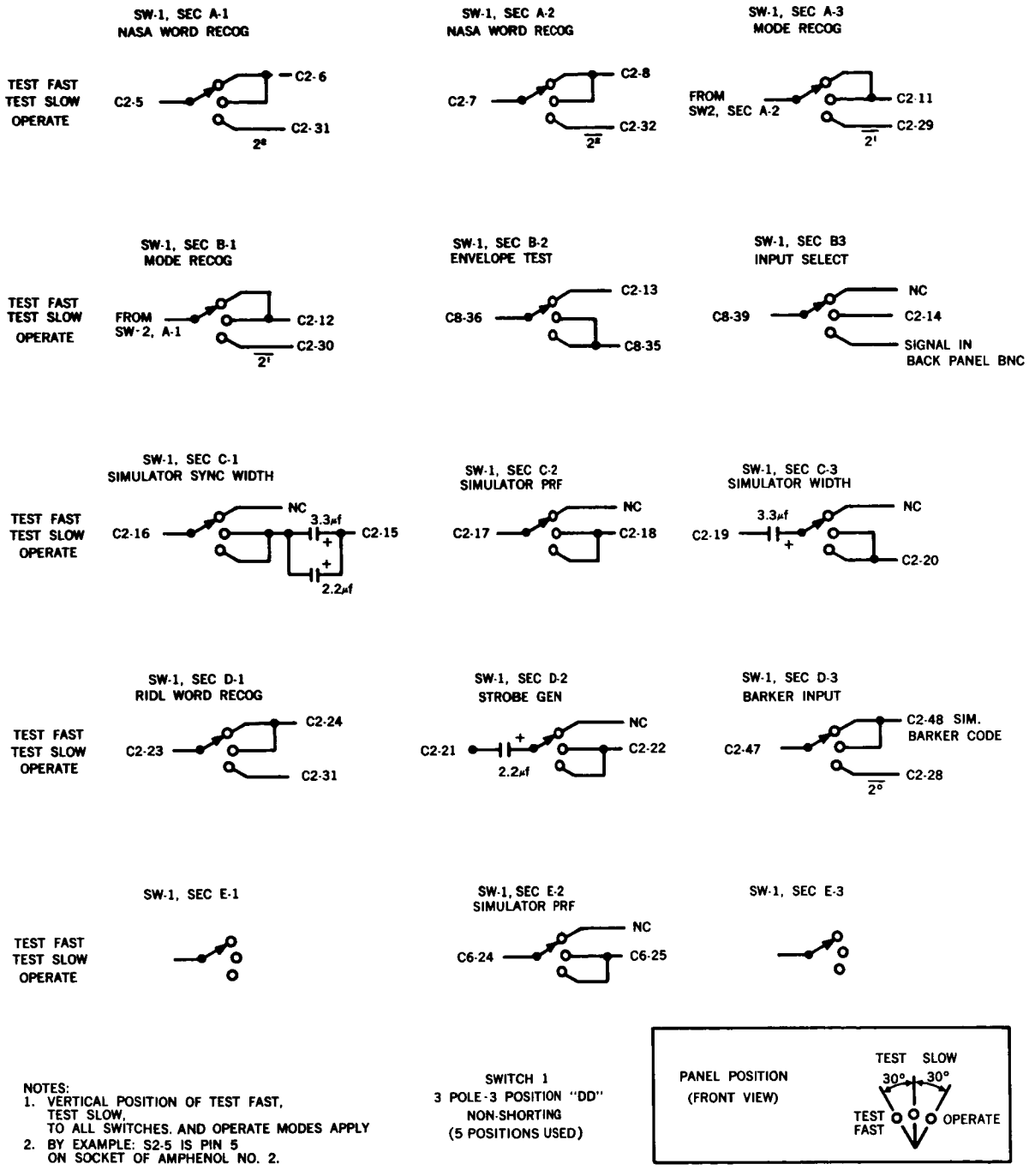
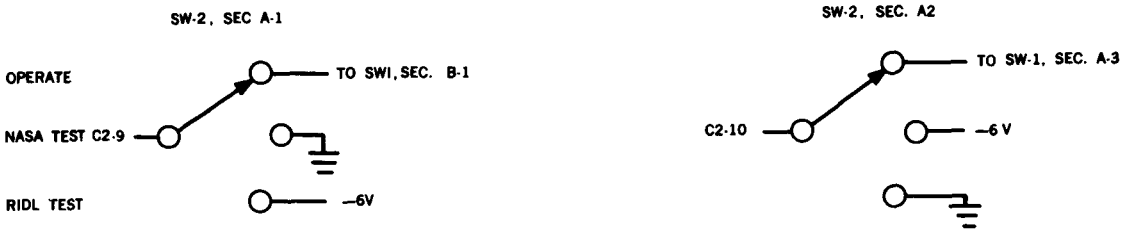
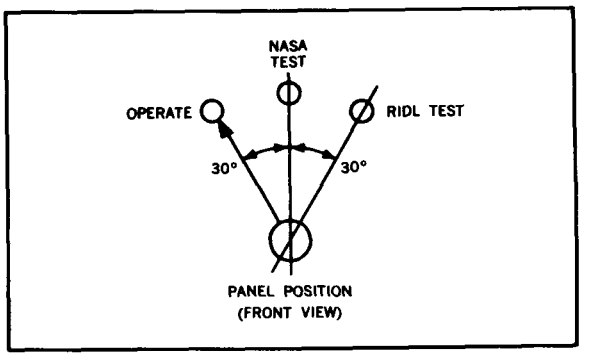


Figure 32–Switch 1 interconnections

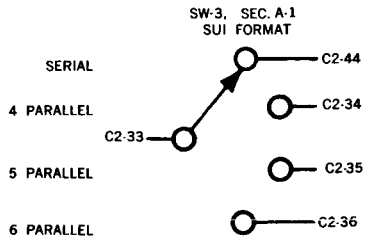


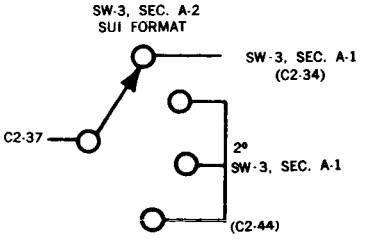
SWITCH 2
2 POLE—5 POSITION "DD"
NON-SHORTING (3 POSITIONS USED)

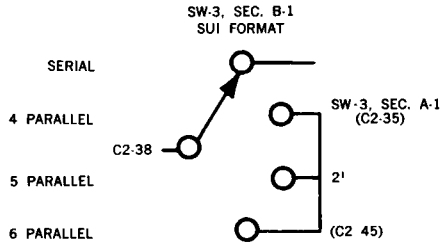


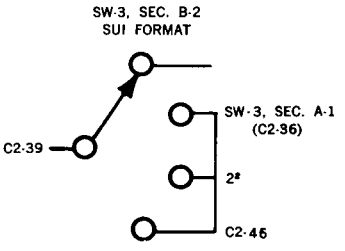
Note: The connection here is to indicate, for example, pin 9 on the socket of amphenol 2 by the symbol C2-9.

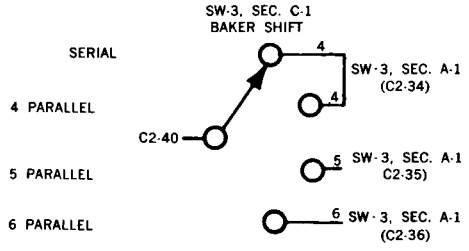
Figure 33—Switch 2 interconnections

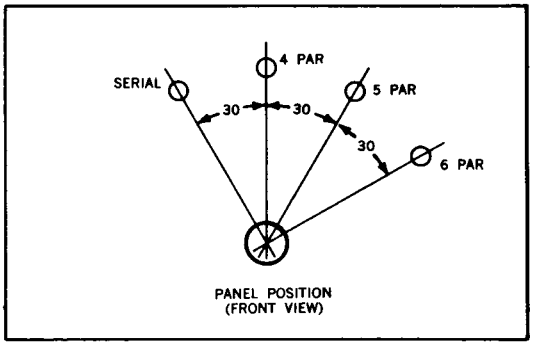












SWITCH 3
2 Pole—5 POSITION "DD"
NON-SHORTING (4 POSITIONS USED)

Note: The convention here is to indicate, for example, pin 44 on the socket of amphenol 2 by the symbol C2-44.

Figure 34—Switch 3 interconnections

SECTION 7
OPERATING PROCEDURES

The normal operating procedures necessary to reduce data directly from the demodulated receiver signal will be described first. Following this will be a discussion on operating procedures for additional uses of subunits within the equipment.

NORMAL OPERATING PROCEDURES

In normal operation, there are no external front panel connections on the Decommutator, Comb-Filter, or the main control panel. Only the two commercial counters will have external front panel connections (see section on counters). Back panel external connections may be seen in Figure 35.

Main Control Panel

1. Throw power switch to ON.
2. Turn OPERATE-NASA TEST-RIDL TEST switch to OPERATE.
3. Turn TEST FAST-TEST SLOW-OPERATE switch to OPERATE.
4. Turn SUI FORMAT switch to that mode employed by the SUI experiment. The SERIAL mode is that mode for which channel 4 provides the 2^0 bit, channel 5 provides the 2^1 bit, and channel 6 provides the 2^2 bit. The PARALLEL mode is that mode for which the one selected channel provides all three bits.

Decommutator

1. Throw Decommutator power switch to ON (this switch may remain on since the main panel power switch controls this unit also).
2. Turn CLIPPER controls full CCW.
3. Turn BURST ADJ control full CCW.
4. Throw BURST ADJ switch to HIGH.
5. Turn BLANK ADJ control full CCW.
6. Throw BLANK ADJ switch to HIGH.
7. Throw SYNC ADJ switch to LOW.

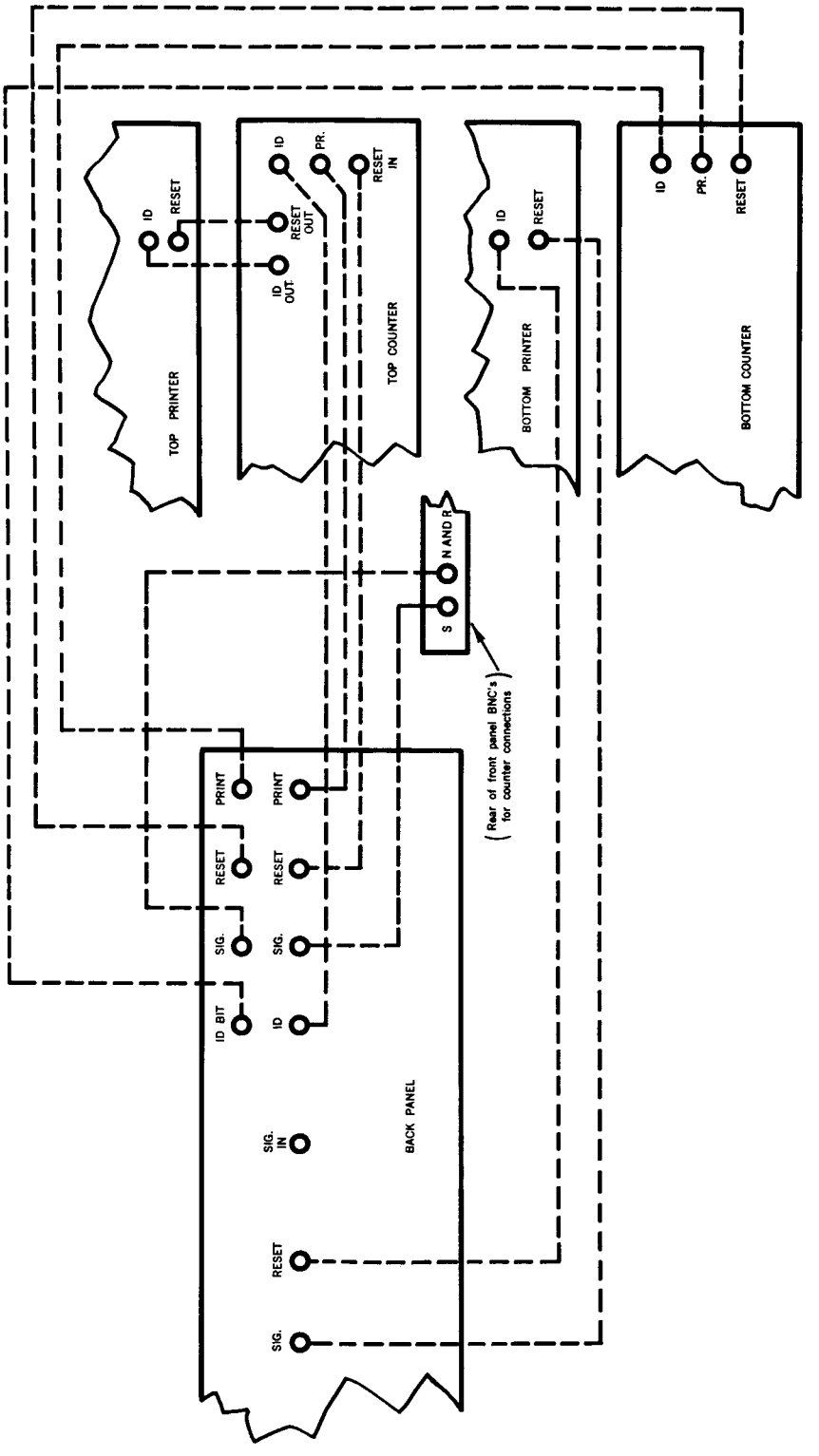


Figure 35—Commercial counter and printer back panel BNC connections

8. Turn SYNC ADJ control full CCW, then by monitoring both FF-3 and the signal at CLIPPER, turn SYNC ADJ control until FF-3 is narrower than the sync burst, but wider than any other burst. The usual setting of FF-3 is for 12.5 msec.

Comb-Filter

1. Throw power switch to ON (This switch may remain on since the main panel switch controls this unit also).
2. Throw TEST-OPERATE switch to OPERATE.

Counters

1. Check rear BNC connections to insure that proper connections have been made; the rear BNC connection may be seen in Figure 35. For data reduction operation three switches, located in the rear of each counter, must be thrown in the upward direction (marked S-3). The internal oscillator switch is one of these switches, the other two are added double-throw switches.
2. Throw rear switches as explained in step 1.
3. Apply signal from main unit to SIGNAL INPUT (the normal input for measuring frequency).
4. Turn SENSITIVITY control to center position.
5. Turn FUNCTION SELECTOR to FREQUENCY.
6. Throw POWER switch to ON. All other controls are immaterial for data reduction operation.

Printers

1. Check rear BNC connections to insure that proper connections have been made. The rear BNC connections are shown in Figure 35.
2. Throw POWER switch to ON.
3. Turn SPACE SELECTOR to Position 1.
4. Throw RECORD switch to ON.

OPERATING PROCEDURES FOR ADDITIONAL USES OF SUBUNITS

Main Control Unit

The equipment discussed in this paragraph is the main control unit (Panel and logic section except Comb-Filter and Decommutator).

The simulator may be used for the purpose of checking the Comb-Filter. The frequency within the burst is controlled by the COARSE and FINE controls and will be the same in each burst. The frequency may be monitored at the OUTPUT BNC adjacent to the simulator controls.

The arithmetic unit and the counters may be checked by turning the TEST FAST-TEST SLOW-OPERATE switch to TEST SLOW. In this position, the signal input is excluded from the Decommutator. If the Comb-Filter is set to OPERATE, then the output of the Comb-Filter will be a function of the setting of the simulator frequency and the counters will display the number commensurate with this frequency setting–see Table 3–and if the Comb-Filter is set to TEST, then the output of the Comb-Filter will be a function of the setting of the three Comb-Filter binary switches and the counters will display the number commensurate with these settings. If the OPERATE-NASA TEST-RIDL TEST switch is in OPERATE position, the simulator will simulate a time-shared data reduction between NASA and RIDL. If this same control is set to NASA TEST, then only NASA data reduction will be simulated. Likewise, only RIDL data reduction will be simulated if the control is set to RIDL TEST.

Table 3

Counter Display for Test Slow Mode

Comb-Filter Output			NASA and RIDL Counter		SUI Counter	
2^2	2^1	2^0	NASA	RIDL	Serial	Parallel
0	0	0	000000	700000	000000	000000
0	0	1	104681	721845	262143	037449
0	1	0	209362	743690	000000	074898
0	1	1	314043	765535	262143	112347
1	0	0	418724	700000	000000	149796
1	0	1	523405	721845	262143	187245
1	1	0	628086	743690	000000	224694
1	1	1	732767	765535	262143	262143

The channel strobes used in the main logic unit may be monitored at the indicated BNC's on the rear panel of the unit.

The DECOM outputs provide the frequency burst of each channel on separate BNC's.

ENVELOPE OUT provides an envelope of the demodulated receiver signal.

The 16th FRAME OUT gives an output every 16 frames.

ASPECT OUT provides, in digital form, a voltage equivalent to the binary number presented by the Comb-Filter.

Decommutator

Any channel selected by the OUTPUT SW may be monitored at the OUTPUT BNC. The envelope of the burst, the blank, or the frequency within the burst of the selected channel may be monitored through adjustment of the BURST-BLANK-FREQ control.

Comb-Filter

The three Comb-Filter outputs which provide the states of the 2^0, 2^1, and 2^2 bits may be monitored at the indicated front panel BNC's.

The output states of the three bits may be controlled manually by throwing the TEST-OPERATE switch to TEST. The individual switches for each bit then control the states of the Comb-Filter outputs. This manual setting is usually used for checking the arithmetic unit and the counters. Refer to the Additional Use of Main Control Unit section for the checkout procedure for the Comb-Filter through use of simulator.

SECTION 8

AMPHENOL CONNECTIONS

In Figure 36, the number appearing in each connection box indicates the number given to that Amphenol Connector.

Tables 4, 5, and 6 give the individual pin connections for each connector. The source and destination of each pin and the function with which it is concerned is given in tabulated form. Fox example, by inspection of Table 4, it can be seen that pin 6 of Amphenol Connector 1, which is wired to S-Bloc II, board 21, pin 9, is connected to pin 6 of Amphenol 2 which is wired to Switch 1, wafer A, pin 1. The connection concerns the 2^2 bit of the NASA Word Recognizer.

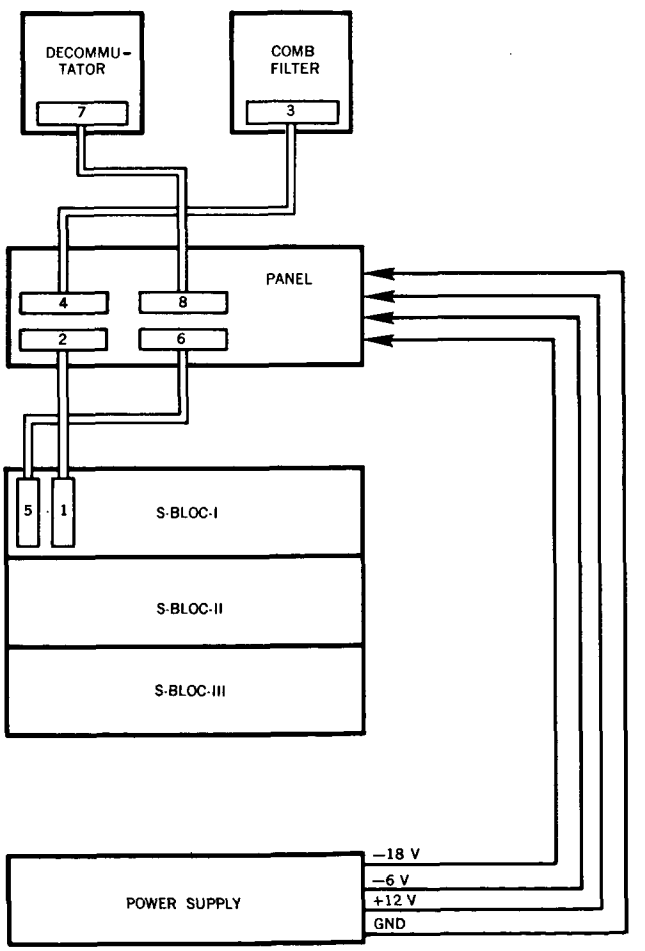


Figure 36—Amphenol and power supply connections (rear view)

Table 4
S-BLOC to Panel Connections*

FUNCTION	S-BLOC BOARD AND PIN NO.	AMPHENOL #1	AMPHENOL #2	PANEL
	GND	1	1	GND
	+ 12v	2	2	+ 12v
	- 6v	3	3	- 6v
	-18v	4	4	-18v
NASA WORD RECOG	II 8-30	5	5	SW-1, A-1
NASA WORD RECOG 2^2	II 21-9	6	6	SW-1, A-1
NASA WORD RECOG	II 8-13	7	7	SW-1, A-2
NASA WORD RECOG $\overline{2^2}$	II 21-6	8	8	SW-1, A-2
N & R MODE RECOG $\overline{2^1}$	II 8-18	9	9	SW-2, A-1
N & R MODE RECOG 2^1	II 8-17	10	10	SW-2, A-2
N - SIMULATOR	II 22-6	11	11	SW-1, A-3
R - SIMULATOR	II 22-9	12	12	SW-1, B-1
ENVELOPE-SIMULATOR	II 20-15	13	13	SW-1, B-2
INPUT SELECTOR SIMULATOR	II 20-20	14	14	SW-1, B-3
SYNC WIDTH SELECTOR	II 7-18	15	15	SW-1, C-1
SYNC WIDTH SELECTOR	II 7-27	16	16	SW-1, C-1
PRF SELECTOR	II 18-28	17	17	SW-1, C-2
PRF SELECTOR	II 18-27	18	18	SW-1, C-2
BURST WIDTH SELECTOR	II 18-10	19	19	SW-1, C-3
BURST WIDTH SELECTOR	II 18-13	20	20	SW-1, C-3
STROBE GEN	II 7-7	21	21	SW-1, D-2
STROBE GEN	II 7-8	22	22	SW-1, D-2
RIDL WORD RECOG	II 12-11	23	23	SW-1, D-1
RIDL WORD RECOG	II 27-33	24	24	SW-1, D-1
		25	25	
	GND	26	26	GND
2^0	II 25-34	27	27	SPARE
2^0	II 25-12	28	28	SW-1, D-3
2^1	II 25-33	29	29	SW-1, A-3
2^1	II 25-23	30	30	SW-1, B-1
2^2	II 25-27	31	31	SW-1, A-1
2^2	II 25-7	32	32	SW-1, A-2
SUI FORMAT	II 17-9	33	33	SW-3, A-1
CHANNEL 4 STROBE	II 4-12	34	34	SW-3, A-1
CHANNEL 5 STROBE	II 4-6	35	35	SW-3, A-1
CHANNEL 6 STROBE	II 4-23	36	36	SW-3, A-1

*NOTE: SW-1, E-1 is wired to SW-1, A-3 and is, therefore, not listed.

Table 4 (Continued)

S-BLOC to Panel Connections*

FUNCTION	S-BLOC BOARD AND PIN NO.	AMPHENOL #1	AMPHENOL #2	PANEL
SUI FORMAT	III 20-10	37	37	SW-3, A-2
SUI FORMAT	III 20-14	38	38	SW-3, B-1
SUI FORMAT	III 20-18	39	39	SW-3, B-2
SUI FORMAT	III 2-16	40	40	SW-3, C-1
FROM COMB-FILTER $\overline{2^0}$	II 25-20	41	41	AMPHENOL #4 PIN-21
FROM COMB-FILTER $\overline{2^1}$	II 25-31	42	42	AMPHENOL #4 PIN-17
FROM COMB-FILTER $\overline{2^2}$	II 25-22	43	43	AMPHENOL #4 PIN-13
TO SUI REGISTER $\overline{2^0}$	II 25-6	44	44	SW-3, A-1
TO SUI REGISTER $\overline{2^1}$	II 25-16	45	45	SW-3, B-1
TO SUI REGISTER $\overline{2^2}$	II 24-21	46	46	SW-3, B-2
BARKER RECOGNIZER	III 12-6	47	47	SW-1, D-3
BARKER RECOGNIZER	II 27-12	48	48	SW-1, D-3
		49	49	
		50	50	

*NOTE: SW-1, E-1 is wired to SW-1, A-3 and is, therefore, not listed.

Table 5

Comb-Filter to Panel Connections

FUNCTION	S-BLOC, BOARD AND PIN NO.	AMPHENOL #3	AMPHENOL #4	PANEL
117v	J-2-2 SW-5-1	1	1	
117v	J-2-2 SW-5-1	2	2	SWITCH ON FRONT PANEL
	TBI-1	3	3	
117v	F1-1 J2-1	4	4	SWITCH ON FRONT PANEL
117v		5	5	
		6	6	
117v TO FAN	TB 1-2	7	7	
GND	11-2	8	8	GND
+8v	11-Y	9	9	
-9v	11-X	10	10	
		11	11	
SIGNAL IN	1-4	12	12	
$-\overline{2^2}$ (INVERTER)	9-U	13	13	AMPHENOL #2 PIN 43
$\overline{2^2}$ (EMITTER-FOLLOWER)	10-U	14	14	
2^2 (INVERTER)	9-T	15	15	
2^2 (EMITTER-FOLLOWER)	10-T	16	16	
$-\overline{2^1}$ (INVERTER)	9-H	17	17	AMPHENOL #2 PIN 42
$\overline{2^1}$ (EMITTER-FOLLOWER)	10-H	18	18	
2^1 (INVERTER)	9-F	19	19	
2^1 (EMITTER-FOLLOWER)	10-F	20	20	
$-\overline{2^0}$ (INVERTER)	9-E	21	21	AMPHENOL #2 PIN 41
$\overline{2^0}$ (EMITTER-FOLLOWER)	10-E	22	22	
2^0 (INVERTER)	9-D	23	23	
2^0 (EMITTER-FOLLOWER)	10-D	24	24	

Table 5 (Continued)
Comb-Filter to Panel Connections

FUNCTION	S-BLOC, BOARD AND PIN NO.	AMPHENOL #5	AMPHENOL #6	PANEL
	GND	1	1	GND
	+12v	2	2	+12v
	-6v	3	3	-6v
	-18v	4	4	-18v
RIDL WORD COUNT	I 17-16	5	5	BNC
RIDL WORD RESET	I 22-16	6	6	BNC
N & R BIT SIGNAL	I 17-7	7	7	BNC
N & R ID BIT SIGNAL	I 25-29	8	8	BNC
16TH FRAME OUT	II 5-7	9	9	BNC
N & R RESET	II 17-16	10	10	BNC
N & R PRINT	II 10-30	11	11	BNC
SUI PRINT	III 9-34	12	12	BNC
SUI RESET	III 9-33	13	13	BNC
SUI ID BIT SIGNAL	III 26-29	14	14	BNC
SUI BIT SIGNAL	III 1-13	15	15	BNC
		16	16	
		17	17	
		18	18	
		19	19	
		20	20	
		21	21	
		22	22	
		23	23	
PRF - SIMULATOR	II 18-29	24	24	SW-1, E-2
PRF - SIMULATOR	II 18-20	25	25	SW-1, E-2
	GND	26	26	GND
	+12v	27	27	+12v
	-6v	28	28	-6v
	-18v	29	29	-18v
DECODER ENVELOPE	II 8-20	30	30	AMPHENOL #8 PIN 44
CHANNEL 0 BURST	II 2-20	31	31	AMPHENOL #8 PIN 27
CHANNEL 7 BURST	II 2-9	32	32	AMPHENOL #8 PIN 28
CHANNEL 2 BURST	II 2-31	33	33	AMPHENOL #8 PIN 29
CHANNEL 3 BURST	II 2-22	34	34	AMPHENOL #8 PIN 30
CHANNEL 4 BURST	II 2-17	35	35	AMPHENOL #8 PIN 31
CHANNEL 5 BURST	II 2-19	36	36	AMPHENOL #8 PIN 32

Table 5 (Continued)
Comb-Filter to Pannel Connections

FUNCTION	S-BLOC, BOARD AND PIN NO.	AMPHENOL #5	AMPHENOL #6	PANEL
CHANNEL 6 BURST	II 2-30	37	37	AMPHENOL #8 PIN 33
CHANNEL 11 BURST	II 2-11	38	38	AMPHENOL #8 PIN 34
FREQ CONTROL (FINE)	II 20-10	39	39	PANEL IK POT
FREQ CONTROL	II 20-8	40	40	PANEL 25 K POT
CHANNEL 0 STROBE	II 26-34	41	41	BNC.
CHANNEL 2 STROBE	II 26-33	42	42	BNC
CHANNEL 3 STROBE	II 26-27	43	43	BNC
CHANNEL 4 STROBE	II 26-12	44	44	BNC
CHANNEL 5 STROBE	II 26-6	45	45	BNC
CHANNEL 6 STROBE	II 26-23	46	46	BNC
CHANNEL 7 STROBE	II 26-7	47	47	BNC
CHANNEL 11 STROBE	II 26-16	48	48	BNC
	BLANK	49	49	BLANK
	BLANK	50	50	BLANK

Table 6

Decommutator to Panel Connections*

FUNCTION	S-BLOC, BOARD AND PIN NO.	AMPHENOL #7	AMPHENOL #8	PANEL
CHANNEL 0 BBF	7-E	1	1	BNC
CHANNEL 1 BBF	7-D	2	2	BNC
CHANNEL 2 BBF	7-F	3	3	BNC
CHANNEL 3 BBF	7-H	4	4	BNC
CHANNEL 4 BBF	7-S	5	5	BNC
CHANNEL 5 BBF	7-T	6	6	BNC
CHANNEL 6 BBF	7-U	7	7	BNC
CHANNEL 7 BBF	7-V	8	8	BNC
CHANNEL 8 BBF	8-E	9	9	BNC
CHANNEL 9 BBF	8-D	10	10	BNC
CHANNEL 10 BBF	8-F	11	11	BNC
CHANNEL 11 BBF	8-H	12	12	BNC
CHANNEL 12 BBF	8-S	13	13	BNC
CHANNEL 13 BBF	8-T	14	14	BNC
CHANNEL 14 BBF	8-U	15	15	BNC
CHANNEL 15 BBF	8-V	16	16	BNC
		17	17	
117v TO FAN	TB1-1	18	18	
117v TO FAN	TB1-1	19	19	
		20	20	
117v	F1-1 J2-2	21	21	117v TO FRONT PANEL SWITCH
117v	J2-2	22	22	
		23	23	
117v	J2-1 SW-5-1	24	24	117v TO FRONT PANEL SWITCH
117v	SW-5-1	25	25	
		26	26	
CHANNEL 0	9-E	27	27	AMPHENOL #6 PIN 31
CHANNEL 7: NOTE	9-D	28	28	AMPHENOL #6 PIN 32
CHANNEL 2	9-F	29	29	AMPHENOL #6 PIN 33
CHANNEL 3	9-H	30	30	AMPHENOL #6 PIN 34
CHANNEL 4	9-S	31	31	AMPHENOL #6 PIN 35
CHANNEL 5	9-T	32	32	AMPHENOL #6 PIN 36
CHANNEL 6	9-U	33	33	AMPHENOL #6 PIN 37
CHANNEL 11	9-V	34	34	AMPHENOL #6 PIN 38

*BBF is a gate pulse occuring at the data burst time of the channel indicated.

NOTE: Channel 1 output in Decoder was changed to provide Channel 7.

Table 6 (Continued)
Decommutator to Panel Connections

FUNCTION	S-BLOC, BOARD AND PIN NO.	AMPHENOL #7	AMPHENOL #8	PANEL
OUTPUT OF BD 1	1-14	35	35	SW-1, B-2
INPUT TO BD II	2-8	36	36	SW-1, B-2
ENVELOP OUT (EF)	6-12	37	37	BNC
AVE SIGNAL TO COMB-FILTER	1-U	38	38	AMPHENOL #4 PIN 12
VIDEO IN	1-6	39	39	SW-1, B-3
		40	40	
	GND	41	41	GND
	GND	42	42	GND
		43	43	
ENVELOP OUT (3 K)	2-6	44	44	AMPHENOL #6 PIN 30
117v TO FAN	TB, 1-2	45	45	
117v TO FAN	TB, 1-2	46	46	
		47	47	
		48	48	
		49	49	
		50	50	

SECTION 9

S-BLOC BOARDS AND THEIR FUNCTIONS

Tables 7, 8, and 9 correlate the physical position of the logic boards in the S-BLOC's and give the function with which each board is concerned.

Also given are the output pins used on each board.

Table 7

S-BLOC Boards and Their Functions

FUNCTION	CIRCUITS USED OUTPUT PIN NUMBER	BOARD	NO.
Blank			1
2^n CTR - 2^0 , 2^1 , 2^3	All	BC	2
Steering NAND's - NASA	All	DN	3
Steering NAND's - RIDL	All	DN	4
2 CTR - 2 , 2 , 2 , 2	All	BC	5
Steering NAND's - NASA	All	DN	6
Steering NAND's - RIDL	All	DN	7
2^n CTR - 2^8 , 2^9 , 2^{10}, 2^{11}	All	BC	8
Steering NAND's - NASA	All	DN	9
Steering NAND's - RIDL	All	DN	10
2^n CTR - 2^{12}, 2^{13}, 2^{14}, 2^{15}	All	BC	11
Steering NAND's - NASA	All	DN	12
Steering NAND's - RIDL	All	DN	13
2^n CTR - ID Bit SUI Barker Print	All	BC	14
Steering NAND's - NASA ID Bit Control Logic - ID Bit	All	DN	15
Control Logic	All	MV	16
Control Logic RIDL Counter, word	All	DI	17
Control Logic Set 0, RIDL word decade	All	DM	18
Control Logic SUI ID Steering	All	DN	19
Control Logic Control Logic - ID	All	FF	20
Control Logic	All	DM	21
Control Logic - ID Bit Word Count, RIDL	All	DI	22
Control Logic	All	MV	23
SUI ID Register	26,27,18	BC	24
Control Logic Master Timer	28,31	DM	25
Blank			26
50 Pin Amphenol			27
50 Pin Amphenol			28

Table 8

S-BLOC #2 Boards and Their Functions

FUNCTION	CIRCUITS USED OUTPUT PIN NUMBER	BOARD	NO.
			1
Strobe Generator	All	DI	2
Strobe Generator	All	DI	3
Strobe Generator	All	DI	4
NASA Word Recognizer	All	DI	5
Strobe Generator Master Timer	All	DI	6
Strobe Generator Simulator	All	DM	7
Strobe Generator NASA Word Recognizer Mode Recognizer (NASA and RIDL)	All	DI	8
Mode Recognizer (NASA and RIDL) NASA Word Recognizer RIDL and NASA Master Timer	All	FF	9
NASA, RIDL Mode Recognizer Master Timer SUI Register	All	PA	10
NASA Word Recognizer	All	PM	11
NASA Word Recognizer NASA and RIDL Master Timer	All	DN	12
NASA Word Recognizer	27,18,6	BC	13
NASA and RIDL Master Timer	All	DM	14
NASA and RIDL Master Timer	All	BC	15
NASA and RIDL Master Timer	All	DI	16
NASA and RIDL Master Timer SUI Register	All	DI	17
Simulator	All	MV	18
Simulator SYNC	All	BC	19
Simulator	All	GO	20
Simulator	All	BC	21
Simulator	All	BC	22
Simulator	All	DN	23
Comb-Filter - $\overline{2^2}$	All	DN	24
Comb-Filter $\overline{2^0}$, $\overline{2^1}$, $\overline{2^2}$ Comb-Filter 2^1, 2^2	All	DI	25
Strobe Generator (for Kruger)	All	DI	26
Simulator Master Timer SUI Master Timer		DI	27
			28

Table 9

S-BLOC #3 (SUI) Boards and Their Functions

FUNCTION SUI	CIRCUITS USED OUTPUT PIN NUMBER	BOARD	NO.
Barker Recognizer Register Control	All	DN	1
Barker Shift Recognizer	All	SR	2
Barker NAND's Counter (timing) Steering	All	DN	3
Barker Recognizer	All	FF	4
21,64 Count Reset Synchronizing Circuit	29,6 28	DM	5
501 Master Timer	All	DN	6
SUI - Master Timer	All	DN	7
501 Master Timer Counter Reset	All	DI	8
Start, Print, Set 0, Timing Gate SUI ID Recognizer Control	All	DI	9
SUI Counter	All	BC	10
SUI Counter SUI Register	All	BC	11
Input Gate to Shift Register SUI Register Steering	All	DN	12
SUI Recognizer	All	BC	13
SUI Recognizer Steering	All	DN	14
SUI	All	BC	15
SUI Steering	All	DN	16
SUI	All	BC	17
SUI Steering	All	DN	18
SUI	All	BC	19
SUI Steering	All	DN	20
SUI Register Control	All	DM	21
SUI ID Register Control	All	DM	22
SUI Register Control SUI ID Register Control	All	FF	23
SUI Register Control SUI ID Register Control	All	DN	24
SUI Register Control SUI ID Register Control	All	DI	25
SUI	All	DM	26
	All		27
	All		28

REFERENCES

1. "Instruction Manual for S-PAC Digital Modules," Publication Number 71-100A, Computer Control Company, Inc., Framingham, Massachusetts, April 11, 1962.

2. Levy, H. H., Demmerle, A. M., and Tinsley, J. L., "A Pulsed Frequency Modulation Decommutation," NASA Technical Note D-1292, June 1962.

3. "S-51, Real-Time Data Reduction System," NASA X-561-62-158, to be published.

BIBLIOGRAPHY

1. "Operating and Service Manual, Hewlett-Packard 523 C/D Electronic Counter," Hewlett-Packard, Palo Alto, California.

2. "Operating and Service Manual, Hewlett-Packard 560A Digital Recorder," Hewlett-Packard, Palo Alto, California.